Digital Time Resolution Limitations of the Domino Ring Sampler as Readout Electronics for Positron Emission Tomography (PET)

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Abstract

Primarily, this doctoral thesis discusses the use of a *Switched-Capacitor Array* (SCA) as an alternative readout electronics for electric signals. Readout electronics is required for example in *Positron-Emission Tomography* (PET) or high-energy physics. To achieve best results from an SCA, some calibrations are mandatory, which are extensively evaluated in this work. In this respect, the *Domino Ring Sampler of the Fourth generation* (DRS4) is investigated in detail. The DRS4 is an SCA and was developed 2007 in Switzerland at the *Paul Scherrer Institute* (PSI). An SCA is basically a ring buffer that stores analog signals very fast in a row. These can be read out at any time in order to digitize the stored signals. Consequently an *Analog-to-Digital Converter* (ADC) sampling in the Megahertz range can be converted into a digitizing system sampling in the Gigahertz range by utilizing an SCA in front of the ADC. Moreover, an SCA distinguishes itself by its favorable cost per channel, the low power consumption and thus the low heat development.

In the course of this work developing a new *Time Calibration* (TC) for SCAs was of of great interest. The new TC-method led to considerable improvement in the time resolution of the DRS4. The time resolution describes the accuracy to determine the temporal distance between two electric signals. Prior to my research, the best TC was offered by the company CAEN from Italy. As a result of this work, the time resolution of the DRS4 improved at least by the factor of 8. Additionally, a time resolution of less than 1 picosecond was reached, which impressively shows the measurement precision of an SCA. The achievement of this excellent time resolution is the result of a special analysis procedure, the cross correlation.

Caused by the improved measurement precision of the DRS4, comparative measurements with other readout electronics solutions became accessible. In addition, new and old technologies are discussed for the analysis of PET signals. At the same time, the main focus was to improve time resolution and simplifying the analysis procedure for PET.

Zusammenfassung

Diese Doktorarbeit erörtert in erster Linie die Verwendung eines *Switched-Capacitor Array* (SCA) als alternative Ausleseelekronik elektrischer Signale, wie sie beispielsweise für *Positronen-Emissions-Tomographie* (PET) oder in der Hochenergiephysik benötigt wird. Um einen SCA optimal zu nutzen, sind einige Kalibrierungen nötig, welche in dieser Arbeit im Detail beleuchtet werden. Dabei wird insbesondere auf den *Domino Ring Sampler der vierten Generation* (DRS4) eingegangen. Der DRS4 ist ein SCA und wurde 2007 in der Schweiz am *Paul Scherrer Institut* (PSI) entwickelt. Ein SCA ist im Wesentlichen ein Ringspeicher, in dem analoge Signale sehr schnell hintereinander gespeichert werden können, um sie zu einem beliebigen Zeitpunkt auszulesen beziehungsweise zu digitalisieren. Folglich kann man durch Verwendung eines SCA, der vor einen *Analog-Digital-Wandler*(ADC) im Megahertzbereich geschaltet wird, einen schnell abtastenden ADC im Gigahertzbereich machen. Ein SCA zeichnet sich außerdem durch seinen günstigen Preis pro Kanal, den geringen Energieverbrauch und die daraus resultierende geringe Wärmeentwicklung aus.

Großes Interesse lag im Rahmen dieser Arbeit auf der Entwicklung einer neuen *Zeitkalibrierung* (TC) für SCA-Chips investiert. Die neue TC führte zu einer erheblichen Verbesserung der Zeitauflösung des DRS4. Die Zeitauflösung steht für die Genauigkeit, mit der der zeitliche Abstand zwischen zwei elektrischen Signalen gemessen wird. Verglichen zu der zuvor besten TC, welche von der Firma CAEN aus Italien angeboten wurde, wurde die Zeitauflösung mindestens um den Faktor 8 verbessert. Eine Zeitauflösung von unter einer Pikosekunde wurde erreicht, was eindrucksvoll die Messgenauigkeit von SCAs verdeutlicht. Um diese sehr gute Zeitauflösung zu erreichen, wurde ein spezielles Analyseverfahren benutzt und weiterentwickelt, die Kreuzkorrelation.

Dank der verbesserten Messgenauigkeit des DRS4 wurden Vergleichsmessungen mit anderen Ausleseelekroniklösungen ermöglicht. Zusätzlich werden neue und alte Techniken für die Analyse von PET-Signalen diskutiert. Im Schwerpunkt stehen dabei eine verbesserte Zeitauflösung und die Einfachheit des Analyseverfahrens für PET.

Contents

List of Figures

List of Tables

List of Acronyms

$\frac{1}{\mu}$	Attenuation Length
Γ	Spatial Resolution
$\Delta t_{a,b}$	Global Time Difference
Δt_b	Local Time Difference
$\frac{\Delta E}{E}$	Energy Resolution
δ_{lin}	Linear Interpolation Error
ΔV_b	Voltage Difference
μ	Mean Value
σ	Standard Deviation
σ_{ce}	Cross Section of the Compton Effect
σ_{pe}	Cross Section of the Photoelectric Effect
A_0	Initial Activity
ADC	Analog-to-Digital Converter
APD	Avalanche Photodiode
ASIC	Application-Specific Integrated Circuit
BGO	Bismuth Germanate
BW	Analog Bandwidth
CAEN	Costruzioni Apparecchiature Elettroniche Nucleari S.p.A.
CAEN-TC	TC-method provided by CAEN
CAEN-VC	VC-method provided by CAEN
CC	Cross-Correlation
CdTe	Cadmium Telluride
Ce	Cerium
CE	Collection Efficiency
CFD	Constant-Fraction Discriminator
CMOS	Complementary Metal Oxid Semiconductor
CRT	Coincident Resolving Time
CRT-test	CRT (FWHM) and $\frac{\Delta E}{E}$ of a PET-Detector Test
c_{stop}	Stop Cell of the SCA
CT	Computed Tomography
CZT	Cadmium Zinc Telluride

DLL	Delay-Locked Loop
DNL	Differential Nonlinearity
DOI	Depth of Interaction
DRS4	Domino Ring Sampler of the Fourth generation
DSC	Domino Sampling Chip
dSiPM	Digital SiPM
e^-	Electron
e^+	Positron
$end\Delta t_b$	Final Set of Δt_b
eV	Electronvolt
EW	Energy Window
$fal\Delta t_b$	Falling Edge Set of Δt_b
FDG	Fluorodeoxyglucose
FOV	Field of View
FPGA	Field-Programmable Gate Array
fs	Femtoseconds
f_{SCA}	Sampling Speed of the SCA
f_{TC}	Frequency which is used for the Time Calibration Signal
FTC	Frequencies Time Calibration
FWHM	Full Width at Half Maximum
FWTM	Full Width at Tenth Maximum
G-APD	Geiger Mode Avalanche Photodiode
GAGG	Gadolinium Aluminum Gallium Garnet
GHz	Gigahertz
GSPS	Gigasamples per Second
GTC	Global Time Calibration
ICC	Interpolated Cross-Correlation
$ini\Delta t_b$	Initial Set of Δt_b
INL	Integral Nonlinearity
K	Kelvin
keV	Kiloelectronvolt
$LaBr_3$	Lanthanum Bromide
LED	Leading-Edge Discriminator
LIDAR	Light Detection and Ranging
LOR	Line of Response
LSO	Lutetium Oxyorthosilicate
LTC	Local Time Calibration
LTC+3GTC	Reference method for NEW-TCs consisting of a LTC + 3GTCs
MAPD	Micro-pixel Avalanche Photodiode
MeV	Megaelectronvolt

MHz	Megahertz
MF	Magnetic Field
mm	Millimeter
MPPC	Multi-Pixel Photon Counter
MRI	Magnetic Resonance Imaging
ms	Millisecond
mW	Milliwatt
MWPC	Multi-Wire Proportional Chamber
n	Index of Refraction
n_{all}	Number of all expected $\Delta t_{a,b}$
NEW-TC	New TC-method developed in this thesis
NEW-VC	New VC-method developed in this thesis
n_{FTC}	Number of FTC frequencies
N_{wave}	Number of waveforms for one distinct TC frequency
N_{decay}	Number of expected decays
NIM-CFD	SIN Constant Fraction Discriminator 102
NIM-LED	LeCroy Leading-Edge Discriminator 623B
NIM-TAC	Tenneelec Time-to-Amplitude Converter TC 861A
ns	Nanosecond
n_{SCA}	Number of SCA cells
NO-TC	Assumption of Equidistant Sampling Points
NO-VC	Absence of VC-methods
P-test	Period Test
P417	Phillips NIM Pocket Pulser model 417
PC	Personal Computer
PCB	Printed Circuit Board
PCC	Precise Cross-Correlation
$PbWO_4$	Lead Tungsten
PDE	Photon Detection Efficiency
PDPC	Philips Digital Photon Counting
PE	Photoelectric Absorption Probability
PET-INSERT	Second Generation Dedicated MR-Compatible Small Animal PET-Insert
PET	Positron-Emission Tomography
PIN	Positive Intrinsic Negative
PLL	Phase-Locked Loop
PMT	Photomultiplier Tube
ps	Picosecond
PSI	Paul Scherrer Institute, Switzerland
PTFE	Polytetrafluoroethylene

QE	Quantum Efficiency
$res\Delta t_b$	Resulting Set of Δt_b
$ris\Delta t_b$	Rising Edge Set of Δt_b
RMS	Root-Mean-Square
RPC	Resistive Plate Chamber
S20	Teledyne LeCroy WaveRunner 640Zi Oscilloscope
S5	LeCroy WaveRunner 6050A Oscilloscope
SCA	Switched-Capacitor Array
SiPM	Silicon Photo Multiplier
SNR	Signal-to-Noise Ratio
SP	Sampling Point
SP-test	Split Pulse Test
SPTR	Single Photoelectron Time Resolution
SSPD	Solid State Photon Detector
SSPM	Solid State Photo Multiplier
t_{FTC}	Equidistant Period Difference
$t_{\max}$	Maximum Calibration Range
$T_{1/2}$	Half-life
TAC	Time-to-Amplitude Converter
TC	Time Calibration
TDC	Time-to-Digital Converter
TH	Threshold
TOF	Time of Flight
TTL	Transistor-Transistor Logic
TTS	Transit Time Spread
T_{SCA}	Elapsed Time for one SCA Rotation
u_{cor}	Correction Unit
V_{cal}	Applied DC-Voltage for VCs of SCAs
v_{cor}	Correction Value
USB	Universal Serial Bus
V_{FTC}	Tolerance Voltage for the FTC
V3	DRS4 Evaluation Board version 3
V3-TC	TC-method provided by the V3
V3-VC	VC-method provided by the V3
V5	DRS4 Evaluation Board version 5
V5-TC	TC-method provided by the V5
V5-VC	VC-method provided by the V5
VC	Voltage Calibration
V_{max}	Symmetric Voltage limit for the TC signal
W2571	Tabor Waveform Generator Model WW2571A

W3251	Tektronix Arbitrary/Function Generator AFG3251
X742	742-Series Board Based on DRS4-chip from CAEN
Z_{eff}	Effective Atomic Number

Chapter 1

Background and Introduction

1.1 Structure of This Work

This work contains five chapters and the appendix. Chapter 1 is inspired by my master thesis [1], the PhD thesis from Pichler [2] and the book of Knoll [3]. Section 1.2 starts the background overview with a general explanation of *Positron-Emission Tomography* (PET) and its applications. The following 9 sections provide deeper insides about PET starting with the physics of the *Positron* (e^+) which is the associated antimatter particle of the *Electron* (e^-). The concept of a PET-detector, consisting of a scintillator, a photodetector and a readout electronics will be described in detail. Basic terms for PET, like *Time of Flight* (TOF), *Depth of Interaction* (DOI) and *Energy Resolution* ($\frac{\Delta E}{E}$) will be introduced. Also time resolution (section 1.6), which is a core theme, will be explained extensively.

If the basics of PET are already present it is recommended to continue reading from the motivation (section 1.11). It introduces the importance of this work with respect to time resolution using fast readout electronics for PET.

In chapter 2 all investigated readout electronics will be introduced. Besides the standard readout electronics, an alternative technology - the *Switched-Capacitor Array* (SCA) - will be provided, which was investigated and improved in the process of this thesis. The chapter ends with a description of all performed experiments utilizing readout electronics.

Chapter 3 provides a comparison between all tested readout electronics. In this

respect the SCA-based boards have been tested under two conditions, the old *Time Calibration* (TC) including the old *Voltage Calibration* (VC) compared to the *New TC-method developed in this thesis* (NEW-TC). Ultimately, an evaluation of all investigated PET-detectors utilizing different readout electronics is presented.

Chapter 4 discusses the results of the previous chapter 3, underlining the possible improvement for SCA-based boards when taking advantage of the NEW-TC. Chapter 4 closes with a discussion concerning all tested readout electronics with regards to PET-detectors.

Chapter 5 provides a résumé of this work, by summarizing the key aspects. An outlook is also given for possible improvements with respect to time resolution for PET and the SCA technology.

Appendix A, covers an international patent and a scientific publication relating to a simplified fraction of the five chapters.

1.2 Positron-Emission Tomography (PET)

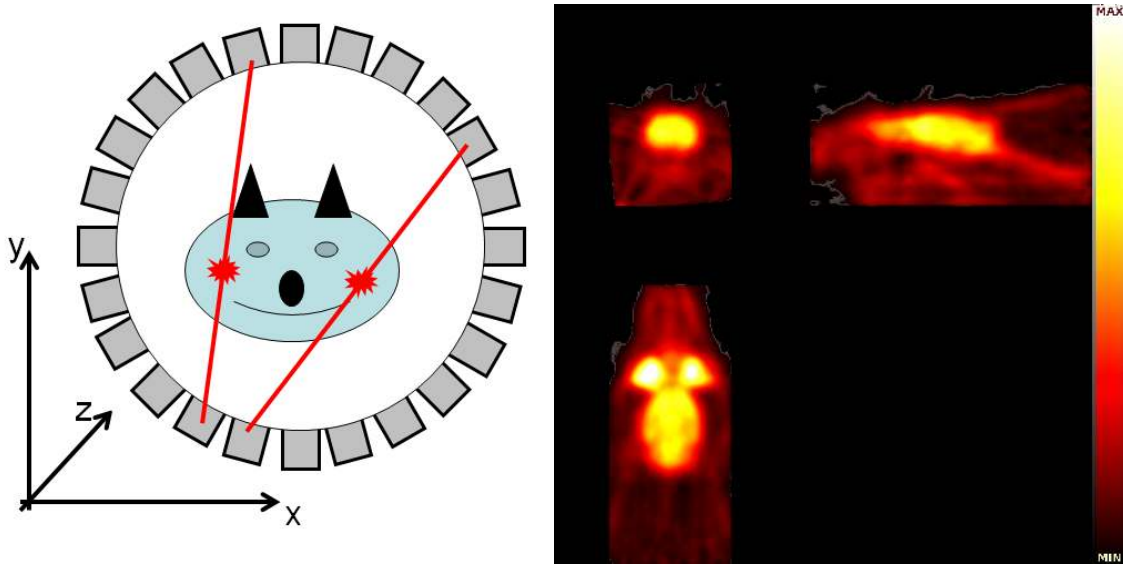
PET is a three-dimensional imaging modality that provides information about molecular processes of living organisms. There are several applications in the clinical routine that benefit from PET. One example is oncology where PET became a reliable appliance to detect cancer. PET can measure picomolar concentrations of radiolabeled molecular probes in vivo [4]. Thus, PET requires about one order of magnitude less concentration of traceable molecules, the so called tracers, compared to alternative imaging modalities such as *Magnetic Resonance Imaging* (MRI).

The general principle of PET-tracers was known already in the year 1923 [5]. A PET-tracer is usually a biologically active molecule labeled with a positron emitting isotope (β^+ decay, more details in section 1.3). Based on the molecule, they are used to investigate tracer-specific metabolism, receptor expression or functional processes of living objects[6]. Since the labeled concentrations are so small, they do not influence the investigated biological systems, but "trace" physiology or pathophysiology in vivo. There is a variety of different PET-tracer available. In most cases the PET-tracer is injected into the living object intravenously. In clinical diagnostics,

especially in the realm of oncology, the most common tracer is the glucose-analogon *Fluorodeoxyglucose* (FDG) which is normally labeled with the isotope ^{18}F [7].

Results using positron emitting particles to detect brain cancer were first published in the year 1951 [8]. However, it took another 24 years before the first PET-scanner was developed [9]. A detailed history of how the PET technology developed is published by Wagner [10].

A PET-scanner consists of at least two opposing PET-detectors that are sensitive for 511 *Kiloelectronvolt* (keV) photons. To yield 3D images, the PET-detectors need to be rotated around the object or more practically several PET-detectors are arranged in a ring expounding transaxially and axially, to enable fast acquisition times at high count rate statistics. PET-detectors consist of selected γ-ray scintillators in combination with fast low noise photodetectors. One of the main challenges for PET-detectors is to guarantee excellent stopping power, optimal time resolution and good energy resolution. Usually, several photodetectors with scintillators are combined together to form blocks, which reduce electronic readout-channels. The detector-blocks are arranged in a ring structure and detect radioactive decay of the PET-tracer over time. Every time two 511 keV photons from one positron-electron annihilation are measured within a pre-defined time window (also called "coincidence window") at two opposing PET-detectors, they are recorded as one coincident event and are subsequently used for image reconstruction. These coincident events correspond to a certain *Line of Response* (LOR) and are illustrated in fig. 1.1(a). Every time a coincident event is recognized, its corresponding LOR gets one additional count. The amount of possible LORs in a PET system depends on the number of crystals, which basically are the number of detection points. The PET-scanner which was tested in this work, consists of 10800 crystals. In theory it would result in 10800^2 LORs for a fully 3D reconstruction. In practice it is reduced by the choice of the reconstruction method and the pre-defined geometrical settings (e.g. *Field of View* (FOV)...[2]). The number of total counts that are detected in a PET-scan depends on the amount of radioactivity in the FOV, the dimensions of the PET-scanner, the solid angle coverage and the scan time. However, by using the information of the LOR-hits, a reconstructed image can be calculated like in



(a) Drawing of a PET-detector ring

(b) PET images of a rat brain

Figure 1.1: (a) shows a schematic of a PET-detector ring at reduced complexity with only 24 PET-detector elements arranged in a ring. It shows further two coincident events which originate from two independent positron-electron annihilation. The red lines represent the LORs connecting the PET-detector pairs. It also symbolizes the trajectory of the opposing gamma rays. (b) shows an exemplary reconstructed PET-image of a rat head (transversal on the left, sagittal on the right and coronal view at the bottom). The rat is injected with the glucose analog ^{18}F-FDG. The image clearly depicts regions of the brain which have a high glucose metabolism.

fig. 1.1(b), where FDG was injected into a rat and a one hour dynamic scan was performed. PET images like in fig. 1.1(b) ordinates from the field of preclinical imaging, where PET became an essential research tool over the last decades. Since the *Spatial Resolution* (Γ) is typically only 1-3 millimeters it became mandatory to combine PET-images with *Computed Tomography* (CT) or MRI to yield anatomical landmarks along with the molecular information as described by Wehrl et al [11].

The image in fig. 1.1(b) was measured with the *Second Generation Dedicated MR-Compatible Small Animal PET-Insert* (PET-INSERT), which is an in-house development. The PET-INSERT typically detects about 3-4 % of all decays, a comparatively high detection sensitivity compared to other dedicated PET-scanners [12]. Additionally, to make use of a detected decay, it has to origin from a coincident event within a possible LOR. The PET-INSERT achieves a Γ of around 1.4 mm *Full Width at Half Maximum* (FWHM) in the center field of view. Γ is limited by the crystal

size, the e^+-energy and the PET-ring diameter[2].

Principally a PET system is able to detect many coincident gamma events per second that originate initially from β^+ decays. The image in fig. 1.1(b) for example was reconstructed from around 10 million coincident events which are measured in the last 15 min of a one hour scan. An *Initial Activity* (A_0) of about 3.7×10^7 Bq was used in the scan. With $T_{1/2}$ of ^{18}F which is around 110 minutes and (1.5) one can calculate that *Number of expected decays* (N_{decay}) is around 24 billion. Thus, the collected events that are used for this brain-image result in less than 0.1 % of the available decays. A mentionable portion of the ^{18}F is also located in the rat-body and produces noise from outside of the FOV scattered γ-rays, detected by the PET-INSERT.

A lot of research happened over the last decades improving PET imaging but there is still room for more:

Scattered events can result in wrong LOR when the direction of γ-rays are changed through Compton scattering[3]. In this case the involved particles undergo a momentum change, which changes the initial direction of the γ-ray. This momentum change of a γ-ray causes a change of the γ-energy. Depending on the $\frac{\Delta E}{E}$ of the PET-detector one can measure the effect of Compton scattered events.

If the exact location of the crystal-hit is to be known, novel PET-detector concepts are needed and are already published. A very promising candidate, providing the mentioned DOI information, is described by Kolb et al [13].

The time window of PET scanners is mainly caused by, the performance parameter, the time resolution. Thus, the time resolution is of central interest in PET technology development as it determines the quality of the reconstructed image. If PET-detectors yield a good time resolution, ideally in the pico-second range, the time window can be kept short and subsequently the detection of random coincident events from two independent electron-positron annihilations can be minimized, which reduces the background noise of the PET-image. Additionally, less radioactivity and scan time is needed which in turn saves costs and reduces the radiation exposure of the patient. At the same time higher doses of activity can be injected if the time resolution is improved. This is especially relevant for tracers consist-

ing of short living radio isotopes where the scan time is only a few minutes like in ^{15}O-studies [14].

1.3 Beta Decay

There are 3 main types of radioactive decays, which are the emission of alpha (α) particles, beta (β) particles and gamma (γ) rays. In PET only the β^+ decay is of interest, where the weak interaction converts the parent nucleus (P) into the daughter nucleus (D) while emitting an e^+ and an electron neutrino ν_e:

$$ {}^{A}_{Z}\mathrm{P} \rightarrow {}^{A}_{Z-1}\mathrm{D} + \mathrm{e}^+ + \nu_\mathrm{e} \tag{1.1} $$

Z stands for the atomic number and defines the element name by providing the amount of protons in the nucleus. A is the mass number and basically the average number of nucleons that form the nucleus[I]. At the fundamental level the β^+ decay is explained by the standard model [15] where an up quark (u) is converted into a down quark (d).

$$ \mathrm{u} \rightarrow \mathrm{d} + \mathrm{e}^+ + \nu_\mathrm{e} \tag{1.2} $$

^{18}F is the most common PET isotope and follows in more than 96 % the β^+ decay, one can predict with (1.1) the outcome, as:

$$ {}^{18}_{9}\mathrm{F} \rightarrow {}^{18}_{8}\mathrm{O} + \mathrm{e}^+ + \nu_\mathrm{e} \quad . \tag{1.3} $$

A decay will only take place if the nucleus can change to an advantageous energy state. In such a case the nucleus will lose mass. The energy of the mass-loss is contained in the kinetic energy of the particle that exits the nucleus, while it is

[I] Nucleons consist of protons and neutrons forming the atomic nucleus and are held together by the nuclear force (strong force).

decaying. Applying Einstein's formula [16][II] combined with the mass difference of $^{18}_{9}\mathrm{F}$ and $^{18}_{8}\mathrm{O}$, which is $\Delta m = 0.00178 \pm 0.000016\,\mathrm{u}$ [17], one will result in an energy-loss of the parent nucleus of $\Delta E = 1.658 \pm 0.015$ *Megaelectronvolt* (MeV). Two energetically equal parts have to be subtracted from ΔE. One part is used for mass production of the e^+ and the other subtraction is caused by the losing of the ninth surrounding e^-. The remaining energy ($\Delta E - 2 \times 0.511\,\mathrm{MeV}$) is mainly split between ν_e and e^+ [18] as kinetic energy ($\Delta E_\mathrm{kin} = 0.636 \pm 0.015\,\mathrm{MeV}$). According to Fowler [19], the maximum kinetic energy of the e^+ from the ^{18}F-decay is 635 keV, which is inside the standard deviation of the above calculated ΔE_kin. The E_kin of the e^+ is one of the factors limiting the Γ of an PET-image, because the e^+ has to lose almost all of its kinetic energy before it can annihilate (see section 1.4). A E_kin of 635 keV corresponds to a maximal e^+-range of 2.3 *Millimeter* (mm) in water. Thus, the maximum error caused by ^{18}F is 2.3 mm for a single PET-measurement. However, since E_kin is split between ν_e and e^+ which in turn scatters in 3 dimensions, the average e^+-range is less. It is described by the point spread distribution and shows for the ^{18}F-decay in water a positron range of 0.1 mm (FWHM) and 1 mm for the *Full Width at Tenth Maximum* (FWTM) [18] & [20].

A radioactive decay is a Poisson distributed process. Thus, one cannot know the exact time point when the radionuclide is decaying. However, one can predict the expected amount of decays at a given time as:

$$A(t) = A_0 e^{-\lambda t}, \tag{1.4}$$

where the A_0 is measured in decays per second (Bq). λ is defined as $\lambda = \frac{ln(2)}{T_{1/2}}$. The *Half-life* ($T_{1/2}$) is the time it takes for a radioactive substance to decay to half of its initial radioactivity. Consequently, the antiderivative of (1.4) results in the N_decay

[II] $\Delta E = \Delta m \cdot c^2 \div e$, one will result in remaining energy ΔE with the unit *Electronvolt* (eV), using:

elementary charge: $e \approx 1.602 \times 10^{-19}\,\mathrm{C}$

unified atomic mass unit: $\mathrm{u} \approx 1.661 \times 10^{-27}\,\mathrm{kg}$

speed of light: $c \approx 2.998 \times 10^{8}\,\frac{\mathrm{m}}{\mathrm{s}}$

between time point a and b:

$$N_{\text{decay}}(a,b) = \int_a^b A(t)\,\mathrm{d}t = -\frac{A_0}{\lambda}\left(e^{-\lambda b} - e^{-\lambda a}\right). \tag{1.5}$$

1.4 Positron-Electron Annihilation

The interaction of matter with its antimatter is called annihilation. It will result in total destruction of the involved masses which in turn are converted into energy. Since energy is a conserved quantity the sum of all involved energies will form new particles as long as the conservation laws are not violated.

In PET, the e^- and the e^+ produce a low-energy annihilation which favors photon production. Photons are particles and simultaneously their behavior can be described with Maxwell's equations [21]. That is why historically different names are given during the endeavor of discovering the interaction between matter and the spectrum of electromagnetic waves/particles. The high-energy photons that are detected in PET-scanners are called γ-rays. A γ-ray typically has an energy above 100 keV. There are two mechanisms producing these photons, the direct annihilation and the decay of positronium. The direct annihilation always forms two γ-rays. The positronium is an exotic atom, in which the positron is bound to the electron. So it is very similar to the hydrogen atom where a proton is bound to an electron. When the positronium is decaying, it will either decay in an odd or in an even number of photons, depending on the spin configurations of the two originally involved particles. Because of conservation of momentum there have to be at least 2 photons. However, for PET the dominant ([22], [23], [24]) two-γ decay is of importance

$$e^+ + e^- \rightarrow \gamma + \gamma^* \quad , \tag{1.6}$$

where γ^* and γ decay in an opposite direction angle of 180°. The angle can vary generally not more than 0.5° dependent on the rest-momentum of the involved particles. In the PET-case each of the two γ-rays decays with an energy E_γ, which is half of the total annihilation energy (E_{total}). E_{total} can be calculated with Einstein's

formula [16] and the masses of the involved particles (m_{e^-}, m_{e^+}) as:

$$E_{total} = (m_{e^-} + m_{e^+}) \cdot c^2 \quad \Rightarrow \quad E_\gamma = \frac{E_{total}}{2} = 511\,\text{keV} \quad . \tag{1.7}$$

γ-rays are absorbed by matter. The linear attenuation coefficient μ of the passed material and the path length x of the appendant γ-rays influence the amount of the attenuated γ-rays:

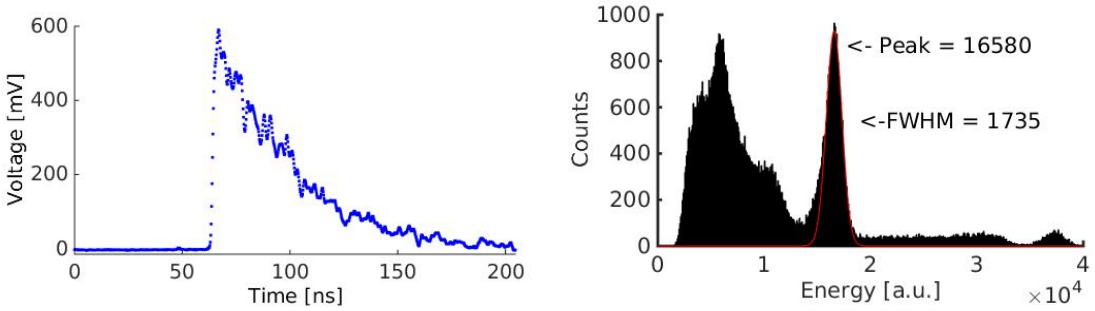
$$I(x) = I_0 e^{-\mu x} \quad , \tag{1.8}$$

where I_0 is the initial intensity. μ also depends on the γ-ray energy which is negligible for PET since 511 keV γ-rays are exclusively used. With (1.8) the absorption in the human body can be predicted. The μ for water lies around $0.1\frac{1}{\text{cm}}$ [25]. Since humans consist in large part of water, one can calculate that 511 keV γ-rays lose around 63 % of its intensity after penetrating 10 cm. In other words, a single 511 keV photon has a 63 % chance to get absorbed by human tissue, after 10 cm. Besides the absorption disadvantages in the human body, the same effect enables PET-detectors to detect γ-rays.

1.5 Energy Resolution ($\frac{\Delta E}{E}$)

A known gamma quantum that is stopped in a state of the art PET-detector, returns a predicable electric signal. The fluctuations of this expected signal results in the $\frac{\Delta E}{E}$ of the PET-detector. $\frac{\Delta E}{E}$ is typically provided as the FWHM divided by its energy of interest. Thus, $\frac{\Delta E}{E}$ describes the reliability of measuring a given energy. Its value is a dimensionless fraction commonly expressed as percentage. Thus, the smaller the value, the better the $\frac{\Delta E}{E}$ [3].

Fig. 1.2(a) shows a single electric signal of a Na-22 event from a PET-detector. The energy of the Na-22 event is represented by the area under the curve. One can see the result of 100,000 such measured Na-22 energies in the spectrum of fig. 1.2(b). The $\frac{\Delta E}{E}$ is $\frac{16580}{1735} = 10.5\,\%$ for the 511 keV annihilation peak, which is a satisfactory result for common PET-detectors. The 511 keV peak is also called photo-peak. The predictable minimum in fig. 1.2(b) lies at two-thirds the photo-peak. It is caused



(a) single Na-22 pulse **(b)** Na-22 spectrum

Figure 1.2: Na-22 spectrum from a typical PET-detector. The utilized PET-detector is described in subsection 2.5.6 (keyword: first experiment).

by Compton scattered γ-rays with energies of $E = 511\,\mathrm{keV}$ and an angle of $180\,^\circ$. All Compton scattered energies are predictable with

$$E' = \frac{511\,\mathrm{eV}}{2 - \cos\theta} \quad , \tag{1.9}$$

where E' is the energy of the 511 keV γ-ray after Compton scattering and θ is the scattering angle. Therefore, the distribution on the left is called Compton continuum. Further, the typical 1.27 MeV peak for Na-22 is also visible in arbitrary units ($\approx 3.8 \times 10^4$). If the energy distribution is gated with a second PET-detector allowing only coincident events from the same annihilation, the 1.27 MeV peak is dramatically reduced and the Compton continuum will form another minimum at one-third the photo-peak resulting from a scatter angle of $90\,^\circ$.

1.6 Time Resolution

Time measurements are normal distributed (also called Gaussian distribution). By repeating an experiment several times one can calculate the *Mean Value* (μ) of the distribution as

$$\mu = \frac{1}{n}\sum_{i=1}^{n} t_i, \tag{1.10}$$

where n is the number of repetitions of the experiment and t_i stands for each measured time.

The excellence of time measurements is described by the width of this distribution

and is usually measured as *Standard Deviation* (σ). Thus, σ provides a number for the fluctuation or measurement reproducibility. For convenience reasons σ is often used as an equivalent for time resolution (also equivalent to: timing, timing resolution or timing results). Improving the time resolution is accomplished when lowering the physical value of σ.

σ can be calculated as

$$\sigma = \sqrt{\frac{1}{n-1}\sum_{i=1}^{n}(t_i - \mu)^2}. \tag{1.11}$$

By using the algebraic formula for the variance, one can modify (1.11) as

$$\sigma = \sqrt{\frac{1}{n-1}\left[\left(\sum_{i=1}^{n} {t_i}^2\right) - \frac{1}{n}\left(\sum_{i=1}^{n} t_i\right)^2\right]}. \tag{1.12}$$

When using (1.12), μ is not needed to calculate σ [26]. This has advantages when computing σ in real time e.g. with a computer program.

The statistical error of the calculated mean value is predicable by the standard error of μ (σ_μ) using σ as

$$\sigma_\mu = \frac{1}{\sqrt{n}} \cdot \sigma. \tag{1.13}$$

Thus, by increasing the measurements (n) one will finally obtain the true μ. Consequently, the smaller σ is, the less n are needed.

1.6.1 Time Resolution for PET-Detectors

The time resolution of a PET-detector consists of several errors which are interrelated as

$$\sigma_{time} = \sqrt{\sigma_a^2 + \sigma_b^2 + \sigma_c^2 + \cdots}, \tag{1.14}$$

in which the overall time error (σ_{time}) is described by the quantities $\sigma_a, \sigma_b, \sigma_c$, etc[III]. In particular, a PET-detector is subdivided in 3 errors:

The 1st error source is the scintillator which stops the 511 keV γ-ray and converts

[III] The errors are always considered to be Gaussian distributed.

it to visible light. It will result in excellent time resolution if it produces a high number of photons in a very short time frame (details in section 1.7).

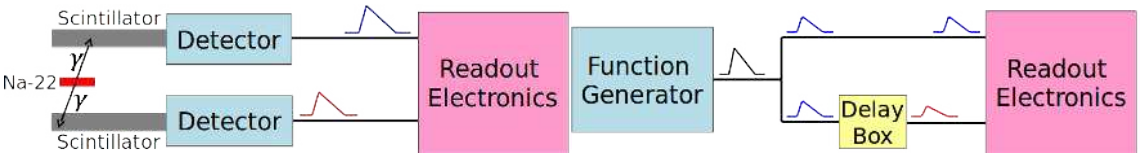
The 2nd error source is the photodetector and limited by the photon detection probability combined with the fluctuation in time converted to an electrical signal. In other words every detected photon produces a predictable time jitter in a photodetector. Consequently, the time resolution will improve when increasing the number of simultaneous photons (details in section 1.8).

The 3rd error source is the time resolution of readout electronics, which is a major topic of this work. It usually contributes little to the overall time error. However, it improves with faster speed, lower electronic noise and intelligent signal processing (details in section 1.9).

To express the time resolution for a PET-detector one uses commonly the term FWHM. The correlation between the previously introduced σ and FWHM can be calculated with the probability density of the normal distribution

$$P(t_i) = \frac{1}{\sigma\sqrt{2\pi}} \cdot exp\left(-\frac{(t_i-\mu)^2}{2\sigma^2}\right), \tag{1.15}$$

to be FWHM $= 2\sqrt{2ln(2)}\sigma \approx 2.36\sigma$. The probability for PET-events to fall in this FWHM-area is around 80 % when calculating its integral with (1.15). The term *Coincident Resolving Time* (CRT) is used as equivalent for PET time resolution[3]. CRT is always given as total time resolution of two PET-detectors measured in coincidence. Fig. 1.3(a) shows a common test setup to investigate the CRT of a PET-detector.



(a) CRT-test setup **(b)** SP-test

Figure 1.3: (a) shows the test setup to measure the total error of a PET-detector. (b) shows a drawing of the SP-test which measures the readout electronics error.

The combined CRT of scintillator, photodetector and readout electronics directly

influences the uncertainty of the determination of the location of annihilation (σ_x) within an LOR as [27]:

$$\sigma_x = \frac{\sigma_t \cdot c}{2}, \tag{1.16}$$

where c is the speed of light and σ_t stands for time resolution (e.g. CRT) of the PET-detector. PET-scanners with a CRT below 1 *Nanosecond* (ns) (FWHM) are usually called TOF-PET. Advanced TOF-PET systems that are used in the clinical routine have a CRT of around 500 ps (FWHM) [28]. The best reported PET-detector shows a CRT of around 100 *Picosecond* (ps) (FWHM) [29, 30]. Thus, when using (1.16) one can predict for such PET-detectors the annihilation position probability with 80 % (because of FWHM) to be inside a 1.5 cm long area within the LOR.

1.6.2 Time Resolution for Readout Electronics

For PET-detectors with a CRT below 100 ps (FWHM) the time resolution of readout electronics will have a major impact. Therefore, it is important to minimize the errors of the input signals in order to find the true time resolution of the readout electronics. The *Split Pulse Test* (SP-test) is an ideal approach for these measurements. The SP-test consists of a pulse, for example coming from a function generator, that is split in two channels. An adjustable delay in the other channel can be used to verify the measured time differences. In fig. 1.3(b) one will find an illustration of the SP-test. The SP-test will reflect the error of the used readout electronics assuming the noise from the function generator to be negligible. This is already the case if the electronic noise of the function generator is one order of magnitude lower than the electronic noise of the readout electronics. By using (1.14) one can calculate that the overall noise increase would be less than 0.5 % for this scenario.

The delay between two split pulses is commonly evaluated by measuring the time difference between the regions with the fastest change over time. For positive signals (or pulses) this is usually the case for the rising edge of the pulse as it is shown in fig. 1.3(b). Faster pulses result in shorter rise times[IV] (t_r) and thus improve the time resolution (σ_t). It is also dependent on the electronic noise (σ_u) and the value of the

[IV] In this thesis t_r is measured from the 10 % to the 90 %-point of A_p. It should be mentioned that the level-crossings to calculate t_r can vary (e.g. t_r from 20 % to the 80 %-point of A_p).

maximum deflection, which is called amplitude (A_p). According to Stricker-Shaver et al [31] these three parameters will provide the expected time resolution by:

$$\sigma_t = \frac{\sigma_u}{A_p} \cdot t_r. \tag{1.17}$$

When working with digitized signals, the simplest approach is setting t_r to the inverse sampling frequency (f_s) of the digitizer (e.g. 5 GSPS results in t_r=200 ps). A_p would then be the average voltage change in the rising edge within t_r[V]. The most common analyzing method is describes by (1.17), which is the 2-points linear interpolation method. σ_t improves with the number (N) of equally relevant *Sampling Point* (SP)s used for the analyzing method by $\sqrt{N}$, for example when using more rising edge points of the pulse to calculate the arrival time.

The values for the time resolution in this thesis are given as "σ" or "FWHM" and refer to resolution on time difference. All these values are extracted from a Gaussian fit applied to their distributions. Often used for a calculated σ, utilizing (1.11), is the terminology *Root-Mean-Square* (RMS). RMS is only identical to σ of a Gaussian fit, if the distribution itself is perfectly Gaussian. Thus, RMS will always be greater than a fitted σ (illustrated in fig. 1.4), unless the distribution of the measurement is not similar to a square function. In this thesis "σ" will refer to the fitted σ of a Gaussian fit and "RMS" to the calculated σ.

In fig. 1.4 one can see that the SP-test results in ≈0.8 ps (σ) which is equivalent to ≈1.9 ps (FWHM). The calculated mean value (μ) is shifted slightly to the left and the calculated standard deviation (RMS) has increased. Both values are influenced by the outliers on the left. Using only the quickly-calculated RMS value has multiple disadvantages such as not knowing if the measured distribution is really Gaussian.

1.7 Scintillators for Gamma Detection

Scintillator crystals are used in PET-detectors to capture γ-rays. The bigger the crystal and the higher the density, the higher the probability to interact with the

[V] The *Analog Bandwidth* (BW) of the readout electronics in combination with signal pulse shape defines t_r[32].

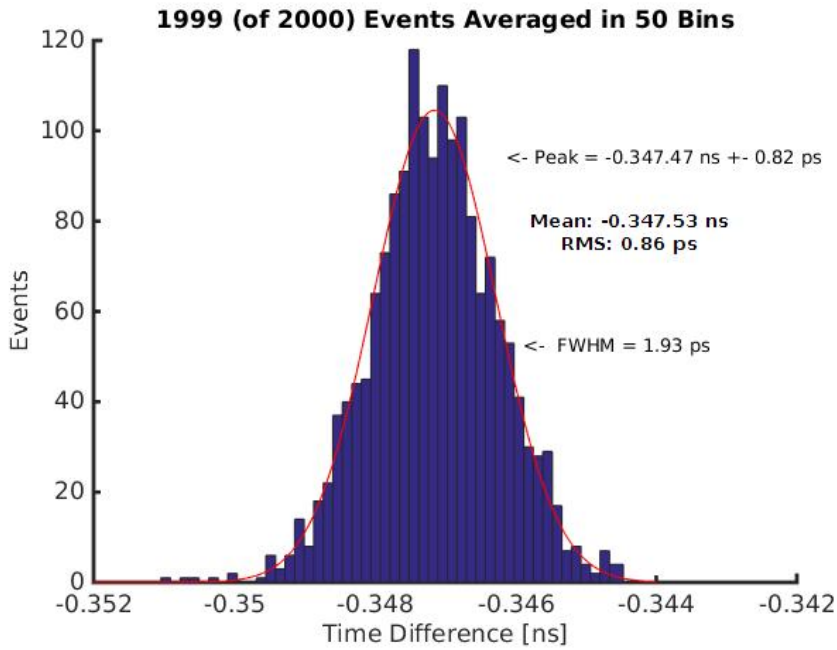


Figure 1.4: Time differences histogram for 2000 arrival times between two signals measured with the SCA-based readout electronics, the *Domino Ring Sampler of the Fourth generation* (DRS4)-chip. The calculated mean is -347.53 ps (μ) with a calculated σ of 0.86 ps (RMS). One event is removed completely because it is more than $6 \times$ RMS separated from μ.

γ-ray. When a γ is interacting, it is converted to many photons of lower energy. These photons are called scintillation-photons and range from visible to ultraviolet wavelengths.

The photoelectric absorption and the Compton scattering are the two mechanisms for capturing γ-rays [3]. The photoelectric effect transfers all energy of the γ to one photoelectron. The e^- in turn will decay from its excited energy state by emitting low energy scintillation-photons. In contrast, Compton scattering converts only a fraction of the γ to the e^-. The remaining energy stays with the scattered photon, as described in (1.9). This scattered photon can still produce additional scintillation centers utilizing both, the Compton or the photoelectric effect. Thus, Compton scattering inside a scintillator result with a high probability in many scintillation centers which makes the position determination challenging.

Therefore the photoelectric effect, which only produces a single scintillation center, is the favored interaction process. It is defined by the *Cross Section of the Photoelectric Effect* (σ_{pe}), which is a function of the density (ρ) and the *Effective*

Table 1.1: List of common PET scintillators with their main properties [33–35].

	BGO	NaI	GSO	LSO	YAP	LuYAP	$LABr_3$	GAGG	$PbWO_4$
peak emission wavelength [nm]	480	410	440	420	350	365	360	520	420
index of refraction (n)	2.15	1.85	1.85	1.82	1.95	1.94	1.9	≈1.9	1.82
light yield [10^3 ph/MeV]	9	41	8	30	17	12	60	57	0.2
decay time [ns]	300/60	230	60/600	40	30	18	16	88/258	15
photon flux [ph/ns at 511 keV]	21	90	60	380	290	340	1,900	600	7
$\frac{\Delta E}{E}$ at 662 keV [%]	10	6	8	10	4.5	15	3	5.2	-
density (ρ)	7.13	3.67	6.71	7.35	5.5	8.34	5.3	6.63	8.3
Z_{eff}	73	50	58	65	33	65	46	54	76
$\frac{1}{\mu}$ at 511 keV [mm]	11.2	25.9	15.0	12.3	21.3	11.0	22.3	?	0.90
PE [%]	44	18	26	34	4.4	32	14	?	?
hygroscopic	No	Yes	No	No	No	No	Yes	No	No
magnetic	No	No	Yes	No	No	No	No	No	No

Atomic Number (Z_{eff}) [VI] of the scintillator. In contrast, the *Cross Section of the Compton Effect* (σ_{ce}) is linearly related to the e^- density ($\sigma_{ce} \propto \rho$). That means, a scintillator should ideally have a large ρ resulting in a high absorption probability and also have a high Z_{eff} for an increased probability of events undergoing the photoelectric absorption. Scintillators are therefore commonly characterized by the *Attenuation Length* ($\frac{1}{\mu}$) [VII] and photo-fraction or *Photoelectric Absorption Probability* (PE)[VIII].

The light yield of a scintillator defines the number of emitted scintillation-photons versus the incident energy (ph/MeV). When dividing 1 MeV by the typically scintillation-light energy of 3 eV (420 nm photon), a theoretical maximum light yield of 330 thou-

[VI] $\sigma_{pe} \propto \rho \cdot Z_{eff}^m$, with the power ($m$) varying dependent on the photon energy between 3 and 4

[VII] $\frac{1}{\mu}$ is the distance into the material where around 37% ($\frac{1}{e}$) of the initial number of particles are left. See (1.8) for more details.

[VIII] PE is the probability that a photon undergoes the photoelectric effect instead of the Compton effect and is defined as $\mathrm{PE} = \frac{\rho_{pe}}{\rho_{pe}+\rho_{ce}}$

sand photons/MeV is achievable. To date the scintillator of choice for PET converts around one-tenth of the initial γ-energy to scintillation-photons. Measuring these photons is Poisson distributed and thus both, CRT and $\frac{\Delta E}{E}$ is inversely proportional to the square-root of the number of measured photons.

Summarized, an ideal PET-scintillator should be non-self-absorptive, have a high light yield and a strong stopping power. Additionally, with respect to a precise DOI information, the photoelectric effect should be the dominate process. It is preferable that the light output is proportional to the initial γ-energy. Otherwise the light output for a full 511 keV energy photoelectric absorption would be different compared to a full energy absorption by multiple Compton interactions. This would result in a degradation of the $\frac{\Delta E}{E}$. The excited scintillator should ideally decay within nanoseconds. A fast decay time is a key aspect of a high count rate and will positively influence the amount of random events. The fast decay time combined with the high light yield enables a huge initial photon number from the scintillator. Such a crystal guarantees an excellent time resolution.

Scintillator crystals can be organic or inorganic. Organic material is generally fast, but has a low light yield. Inorganic crystals have a greater light yield, but are relatively slow. The major properties of common scintillators are given in table 1.1. For more examples and details please read the recommended literature [3, 30, 33–42]. Additionally, three inorganic crystals that are common for commercial PET-scanners and two organic scintillators will be discussed in the following 2 sub-sections.

1.7.1 Organic Scintillators

The most common organic scintillators are solid plastic scintillators. The mechanism in organic crystals is due to the transition in the energy levels of a single molecule. The energy of an incident photon can be absorbed by exciting the electron to a higher state which in turn will quickly fall back to the ground state causing fluorescence.

The scintillators of interest show an energy spacing of 3-4 eV between the ground state S_0 and the first excited state S_1. The higher states are usually somewhat smaller. Each of the states is subdivided into a series of levels with much finer spacing. Because the thermal energy is too low to excite states to one of its finer

energy levels, an organic scintillator is at room temperature in the $S_{0,0}$ state. Furthermore, any state level with vibrating energy (such as $S_{0,1}$, $S_{1,1}$ or $S_{1,2}$) is not in thermal equilibrium with its neighbors and will lose this vibrating energy resulting in the lowest level of its state (e.g $S_{0,0}$, $S_{1,0}$). However, the energy of a fluorescence photon can cause the corresponding electron state to fall to a vibrating level of the lower state (e.g. from $S_{1,0}$to $S_{0,3}$). Because most fluorescence photons will have less energy than the minimum required for excitation (except $S_{1,0}$ to $S_{0,0}$), there is very little overlap between both spectra. This phenomena is called the Stokes shift and causes consequently the self-absorption to be very small [3]. An example of a promising future organic scintillator is *Gadolinium Aluminum Gallium Garnet* (GAGG), where Z_{eff} increases by loading it with elements having high atomic numbers. It has a very high light yield of 60,000 photons/MeV, a good $\frac{\Delta E}{E}$ of around 8 %, a high density of around 6.6 g/cm^3 and no self-radiation. GAGG is expected not only to be a promising scintillator for PET, but also for other gamma camera applications because of its attractive properties [33, 37–39].

1.7.2 Inorganic Scintillators

The mechanism in inorganic crystals is due to the electronic band (layer) structure, separating valence layer and conduction layer by the forbidden energy gap of 3-12 eV. Radiation in the mentioned energy range or higher can excite e^- from the valence layer to the conducting layer. Inorganic scintillators contain impurities caused by doping the crystal. The impurities, so-called activators, create special sites in the lattice with a modified layer structure. These sites provide additional energy states within the forbidden energy gap through which the e^- can tunnel or de-excite back to the valence layer. The available energy of this transition is reduced compared to the forbidden energy gap. The de-excitation sites cause the main luminescence of the scintillator. Additionally, the energy of the de-excitation transition is not enough to lift an e^- from the valence to the conduction layer (no overlap of emission and absorption spectra). Because of these activators, the scintillators are mostly transparent to their scintillation light. Thus, only little self-absorption by the crystal is expected.

To date *Lutetium Oxyorthosilicate* (LSO) which is doped with *Cerium* (Ce) is the most suitable scintillator for PET. Its main properties are available in table 1.1. It combines a high light yield of 30,000 photons per MeV, a high detection efficiency with an $\frac{1}{\mu}$ of 12.3 mm, a high PE of 34 %, a short decay time of 40 ns and a short signal rise time of 0.5 ns [41]. However, the non-linearly behavior in the energy of the light output is a drawback [36]. Another problem of LSO is that lutetium contains by 2.6 % of the radioactive isotope $^{176}_{71}$Lu , which has a $T_{1/2}$ of 40 billion years and undergoes the β^- decay. When $^{176}_{71}$Lu decays, it additionally produces three characteristic γ-energies that often sum to 509 keV, which is indistinguishable compared to PET-events. Both, the kinetic energy of the escaping e^- and the corresponding γ-rays can mimic a PET-event in a scintillator crystal. The background count rate is around 280 counts per second in 1 cm^3 LSO. Since PET-scanners filter out coincidence events, the majority of these events are rejected. For clinical PET the presence of $^{176}_{71}$Lu has very little impact, but certainly, it can effect dedicated small animal PET studies with low count rates [36]. Scintillation properties of LSO can be improved by doping the crystal additionally with Ca^{2+}. An output of around 40,000 photons/MeV is achieved, while the scintillation decay time improves to around 30 ns. However, the pure mechanical properties of LSO:Ca cause a significant fraction of defective crystals in the production process[40].

Lanthanum Bromide ($LaBr_3$) doped with Ce is the material that first achieved a time resolution below 100 ps (FWHM) [29]. It has a high light yield with 60,000 photons/MeV, a short decay time ($\approx$16 ns) and a short rise time ($<$1 ns) [41]. Because of the light yield [42], $\frac{\Delta E}{E}$ is better compared to LSO, resulting in an improved Compton-scatter rejection within tissue. On the other hand, the detection efficiency is half and PE is low compared to other PET-crystals. Thus, more scintillation material is required to obtain sufficient stopping power. Larger crystal dimensions mean more costs and low PE results in an increased Γ. Additionally, the larger crystal size increase the parallax effect. Also, $LaBr_3$ requires dedicated sealing due to its high hygroscopicity.

The scintillator *Bismuth Germanate* (BGO) is one of the few materials not requiring a doping material. The luminescence comes from the Bi^3+ ion. A large

shift between the optical absorption and the emission spectrum causes little self-absorption. It has a high PE, a massive density Z_{eff} and therefore the highest $1/\mu$ value that is used in commercial PET scanners. This leads to the highest detection efficiency for PET, with an 1.6 times higher σ_{pe} than that of LSO [36]. On the other hand its temperature-depending light yield [3] and its decay time of 300 ns are drawbacks compared to other scintillators. The poor decay time and light yield make it a weak crystal for good time resolution, which lowers the count-rate and increases the number of random coincidences due to the need of a wide time window. Because of the low production costs and the high detection efficiency, BGO has been the most widely-used scintillator in previous PET-scanners. To date, LSO replaced BGO and has become the dominate scintillator for PET-scanners.

1.8 Photodetector

The content in the following lines, describing a variety of photodetectors with respect to PET, is mainly influenced with decreasing impact by Vinke [30], Knoll [3], Renker et al [43–46], Lecomte et al [35, 47] and Gerthsen [15] respectively.

A photodetector is needed to convert light into an analog signal. Generally speaking, radio-antennas which are sensitive to low energy photons, are also photodetectors. However, when using the phrase photodetector, visible-light photons or greater photon energies are typically detected. A *Photomultiplier Tube* (PMT) or a *Solid State Photon Detector* (SSPD) are the common choices to detect these photons. For PET applications a scintillator (section 1.7) must be placed before these photodetectors. All photodetectors function identically. The energy of incident photons is transfered to photoelectrons.

PMTs employ the photoelectric effect. Thus, an e^- can be hit out of its energy level from a photon. This photoelectron gets directly amplified multiple times resulting in a measurable current. The initial photon energy must be higher than the binding energy of the e^-, in order to remove the e^- from its energy state completely. Thus, the binding energy of the e^- defines the energy spectrum of the detectable light. Typical PMTs used for PET can detect energies up to 630 nm [44].

More details about PMTs are available in section 1.8.1.

In general, SSPDs consist of silicon which functions as insulators at 0 *Kelvin* (K). If the thermal energy of the e^- increases, the valence e^- can participate in conduction[3]. A photon can also transfer the e^- from the valence to the conduction layer. The layer gap between the valence and the conduction layer is $E = 1.12\,\text{eV}$ at room temperature for silicon. The layer gap defines the lowest possible photon energy that silicon can still detect. One can calculate with[IX]

$$\lambda = \frac{E \cdot h}{c} \quad , \tag{1.18}$$

that this wavelength is around $\lambda = 1100\,\text{nm}$. Silicon can be doped with elements from the 5 th group of the periodic system (e.g. As or P) resulting in an additional free e^- and is then called p-type silicon. By using an element from the 3 rd group of the periodic system (e.g. B or Ga), a defect (positive hole) is created. This doping material is called n-type silicon. Surrounding silicon with n and p regions, results in a basic SSPD-case, the *Positive Intrinsic Negative* (PIN) diode. When applying a reverse voltage, a PIN diode can detect photons. If a photon gets absorbed in the middle (intrinsic) region, it provides the energy to lift an e^- to the conduction layer. At the same time a hole is created in the valence layer. The free charge carriers (e^- and holes), travel to the n or p region which causes a measurable voltage change. A PIN diode has a gain of 1. Some SSPD have an internal gain (gain > 1), which means that they multiply the photoelectron. High gain leads to improved *Signal-to-Noise Ratio* (SNR) and, if high enough, causes a direct measurable electrical current from a single photoelectron. In this case no additional amplifier is necessarily needed.

The typical active area of an SSPD used for PET applications lies around $3\text{x}3\,\text{mm}^2$ with a thickness of only a few μm. Because of the thin active layer, the produced charge carriers travel a small distance. Therefore, a good time resolution can be expected. The thickness and the low atomic number makes it almost invisible for 511 keV γ-rays which is reproducible with (1.8). SSPDs also function inside magnetic fields which made simultaneous PET-MRI scans possible. Since SSPDs can be

[IX] $c \approx 2.998 \times 10^8 \frac{\text{m}}{\text{s}}$ (speed of light)
$h \approx 4.136 \times 10^{-15}\,\text{eV·s}$ (Planck constant)

fabricated in *Complementary Metal Oxid Semiconductor* (CMOS) processes, they are available for relatively low cost. With dedicated SSPDs, the probability to detect visible photons can reach 80 % [43]. Two SSPD-based photodetectors are used in PET-systems which are the *Avalanche Photodiode* (APD) and the *Silicon Photo Multiplier* (SiPM).

Summarized, the PMT, APD and the SiPM are the standard in PET imaging. Some scanners have also used other photodetectors, where a Γ in the sub-millimeter region is targeted. This is particularly an advantage for preclinical small animal imaging. These alternative photodetectors require no scintillator and therefore γ-rays are detected directly. *Cadmium Telluride* (CdTe) [48] and *Cadmium Zinc Telluride* (CZT) [35] are two of the candidates that realize this approach with remarkable $\frac{\Delta E}{E}$ less than 2 % for γ-energies of 511 keV. However, these photodetector types are expensive, they have purity problems and they need dramatic cooling to reduce noise. Also, the time resolution is much worse compared to standard photodetectors and the stopping power is reduced by a factor of 3 compared to standard PET-scintillators. On the other hand, the Γ is interesting for brain imaging or small animal imaging. Brain studies, comparing CdTe and conventional PET scanners, show better tumor identification [49, 50] for CdTe-based scanners because of its higher Γ and better $\frac{\Delta E}{E}$.

Another alternative PET-detector concept using gaseous ionization detectors is the *Resistive Plate Chamber* (RPC) [51] and the *Multi-Wire Proportional Chamber* (MWPC) [52–54]. The idea is that a γ-ray ionizes gas chambers and trigger small avalanches of electrons resulting in a measurable electric signal. Since the ionization energy for gas is about 10 times higher than for semiconductors, the energy information is not satisfactory for the 511 keV events. However, the low construction costs of RPC-detectors, the excellent time resolution of 300 ps (FWHM), a high system sensitivity, sub-millimeter Γ and the DOI information [55] are the main advantages of this technology. MWPC-detectors also result in sub-millimeter resolution, but suffer with respect to time resolution, detection efficiency and count rate performance [35].

The three common photodetectors used for PET are explained in more detail in

the next 3 sub-sections. Their characteristics are summarized in table 1.2.

1.8.1 Photomultiplier Tube (PMT)

PMTs became available in the mid-1930s [56]. Utilizing a PMT as a photodetector is relatively simple, since only a supply voltage has to be applied to receive an analog signal. Fig. 1.5 shows a schematic view of a PMT. One can see that a high-energy photon produces scintillation-photons. A scintillation-photon enters the PMT through a light transmitting window. This photon arrives at the photocathode

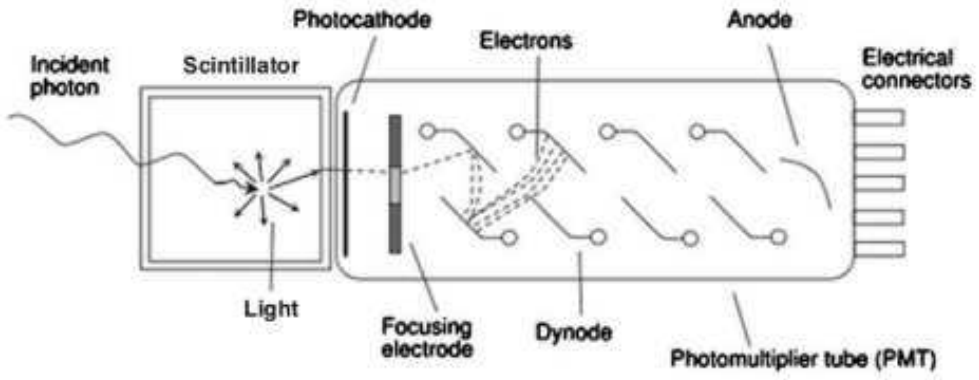


Figure 1.5: Schematic view of a PMT coupled to a scintillator, figure copied from [35].

where it can free an e^-. In this case the e^- accelerates because of an applied voltage potential difference towards the first dynode. It will arrive at a higher energy at this dynode, where low-energy electrons will be freed. These electrons in turn will accelerate towards the following dynode, because of its increased potential difference. This multiplication of electrons is repeated several times until it results in a cascade of electrons which finally arrive at the anode where the current is measured. This current or analog signal can now be processed further (e.g. to compute the arrival time information).

The PMT is sealed in a glass tube. Inside the glass tube is a vacuum which enables electrons to move without interaction with other particles. The transmitting window is also part of a vacuum seal. Borosilicate is commonly used as transmitting material with a thickness less than 1 mm. Due to absorption inside the glass, the sensitivity of a PMT towards high-energy photons is limited. The shortest wavelength that

borosilicate glass still transmits is around 300 nm. However, standard scintillators for PET produce photons with a wavelength around 420 nm (table 1.1). Therefore, most photocathodes for PET that are placed at the inner side of the transmitting window consist of bi-alkali metals which have their maximum sensitivity at 420 nm.

The scintillation-photons (e.g. 420 nm) must travel through different materials before they arrive at the cathode. The *Index of Refraction* (n) of a material which is wavelength dependent has an impact on the amount of arriving photons. The first material is the scintillator which produces the photons. It has an $n \approx 1.9$ for 420 nm. The borosilicate glass of the PMT is one of the last materials before the photons undergo the photoelectric effect. The n of the glass lies around 1.5 for 420 nm. Thus, in this particular case, if the light that is coming from the scintillator exceeds the critical angle of 52°, total internal reflection will take place on the glass surface of the corresponding PMT. This effect is described by Snell's law [15]:

$$\frac{n_2}{n_1} = \frac{\sin\,\theta_1}{\sin\,\theta_2}, \tag{1.19}$$

where n_1 is the index of refraction of the material where the light is momentarily traveling and the n_2 is the index of refraction of the material towards the light is moving. The incident (1) and refracted (2) light that make an angle to the normal of the materials interface are given as θ_1 and θ_2, respectively. Apparently, a critical angle only exists for $n_2 < n_1$. It should be mentioned that before the critical angle is reached ($\theta_2 = 90°$) a fraction of the passing light is reflected. This also remains valid for the ideal case of direct light ($\theta_2 = 0°$). For the mentioned scintillator-borosilicate-example (from $n = 1.9$ to $n = 1.5$) around 1.4 % of the direct entering light will be reflected before entering the PMT glass, where another reflection happens (from $n = 1.5$ to $n = 1.0$) .

The amount of reflected light increases with increasing the incident angle until the light is completely reflected. One has to distinguish between two polarizations dependent on the given incident angle to calculate the intensity of the reflected light.

This is described by the Fresnel equations [15] as

$$R_{\mathrm{s}} = \left(\frac{n_1 \cdot \cos\theta - n_2 \cdot \sqrt{1 - \left(\frac{n_1}{n_2} \cdot \sin\theta\right)^2}}{n_1 \cdot \cos\theta + n_2 \cdot \sqrt{1 - \left(\frac{n_1}{n_2} \cdot \sin\theta\right)^2}} \right)^2$$

and

$$R_{\mathrm{p}} = \left(\frac{n_2 \cdot \cos\theta - n_1 \cdot \sqrt{1 - \left(\frac{n_1}{n_2} \cdot \sin\theta\right)^2}}{n_2 \cdot \cos\theta + n_1 \cdot \sqrt{1 - \left(\frac{n_1}{n_2} \cdot \sin\theta\right)^2}} \right)^2, \tag{1.20}$$

where R_{s} and R_{p} stand for the reflectance with a polarization direction of the light that is perpendicular (s) respectively linear (p) to the plane of incident. θ stands for the angle between the incident light and the normal of the interface. Except for angles close to the critical angle the resulting reflectance ($\frac{R_{\mathrm{s}}+R_{\mathrm{p}}}{2}$) is negligible. When looking at the given scintillator-borosilicate-example again, an incident angle of $\frac{3}{4}$ of the critical angle would cause only around 5 % of the incident light to be reflected. In contrast to the 1.4 % loss of the PMT, 21 % of the direct light is reflected when entering the SSPD ($n \approx 5.1$ for 420 nm) from the scintillator side. Thus, the evacuated glass tube of PMTs looks advantageous compared to the high n of SSPDs which consist of silicon. This is why the entrance window of an SSPD must be coated with a thin anti-reflection layer [57].

Another important parameter of the PMT is its *Quantum Efficiency* (QE). It is defined as the probability that an e^- is freed from the photocathode by a given photon. The QE is a function of the wavelength and depends on the cathode and the transmitting window. PMTs show QE values of around 20-40 % which is approximately two times lower than what can be achieved with SSPD. In order to make a fair comparison between PMTs and the later introduced SSPDs, the *Photon Detection Efficiency* (PDE) will be introduced:

$$\mathrm{PDE}_{\mathrm{PMT}} = \mathrm{QE}(\lambda) \cdot \mathrm{CE}, \tag{1.21}$$

with *Collection Efficiency* (CE) and a wavelength(λ) dependent QE. CE is the ratio of captured photoelectrons at the first dynode compared to the emitted photoelectrons and is typically around 90%.

The dynodes (5-10 dynodes for an average PMT) function as a low noise amplifier and result in a typical gain around 10^6. The noise is caused by the stochastic character of the freed electrons emission [44]. The gain is defined by the potential differences and their corresponding number of dynodes. The anode finally collects the multiplied electrons resulting in a detectable output pulse. Additionally to the anode signal from the PMT, a dynode signal is sometimes available, too. This signal is connected to one of the last dynodes and its amplitude is somewhat lower compared to that of the anode. Since every dynode stage increases the noise, the dynode signal will provide a better time resolution result than the anode signal.

The response time of a PMT is defined by the time required for the photoelectrons to reach the anode after being emitted from the cathode. Its fluctuation, determines the time resolution and is also known as the *Transit Time Spread* (TTS). Increasing the supply voltage improves the electron traveling speed and therefore shortens the TTS. Thus, the TTS depends on the supply voltage of the PMT and improves inversely proportional to the square root of the voltage.

The disadvantage of a PMT compared to a SSPD is its relatively low PDE of 20-40 %, its large size and its sensitivity to magnetic fields. Since PMTs are bulky, they are often applied if large packing space is available and large active areas need to be covert. The sensitivity to magnetic fields make PMTs useless for simultaneous PET-MRI scanners. On the other hand, low dark current and high gain are the major advantages for PMTs. The high gain in combination with the fast rise time means that no additional amplification is needed. Therefore a PMT is easier to use compared to an SSPD and an ideal candidate for preliminary tests.

1.8.2 Avalanche Photodiode (APD)

The first SSPD used for PET application was an APD [47, 58]. APDs have an internal gain of 10^2-10^3 and usually run in reach-through mode. APDs consist of a thin p++ layer, a wide depleted drift region followed by the p and n+ regions (avalanche

Table 1.2: Comparison of photodetectors with their main properties for PET. The table is adopted from [35].

	PMT	APD	SiPM
Operation voltage [V]	1000-2000	100-1500	30-80
Gain	10^5-10^7	10^2	10^5-10^6
Active area	1-2000 cm^2	1-100 mm^2	1-10 mm^2
Dynamic range	10^6	10^4	10^3
Rise time [ns]	<1	2-3	≈1
Time jitter (FWHM) [ns]	0.3	>1	0.1
Dark current / counts	<0.1 nA/cm^2	1-10 nA/mm^2	0.1-1 MHz/mm^2
PDE (λ=420 nm)	<40%	<80%	<50%
Temperature coefficient	1 %/°C	2 %/°C	4 %/°C
Magnetic susceptibility	>5 mT	up to 9.4 T	up to 15 T

region). The drift region is also called intrinsic or π region with a thickness ranging around 100 μm [59]). Thus, it is similar to a PIN diode, except for the additional placed avalanche region whose impact is dependent on the reverse bias voltage. This voltage can vary from 100 V to 1000 V. Thus, at a low bias voltage the APD will function as a PIN diode.

In fig. 1.6 one will find the illustrated APD functionality. The avalanche region has a high doping concentration. This causes a high electric field in this region when the reverse bias voltage is applied. Photons that enter the π region, will produce electron-hole pairs. The electric field attracts the e^- towards the avalanche region. The electric field causes an e^- to receive energies greater than the ionization energy of silicon resulting in secondary e^- and so on. This procedure is called the avalanche effect and operates as the internal gain process in an APD. The best SNR will be achieved from a typical gain of around 100 which is 10 thousand times lower compared to the gain of a typical PMT. Consequently, the electronic noise of the APD is relatively high compared to the signal amplitude. Additionally, an APD also has a high statistical variation on this gain. The gain strongly depends on temperature and varies exponentially with the applied bias voltage. The gain

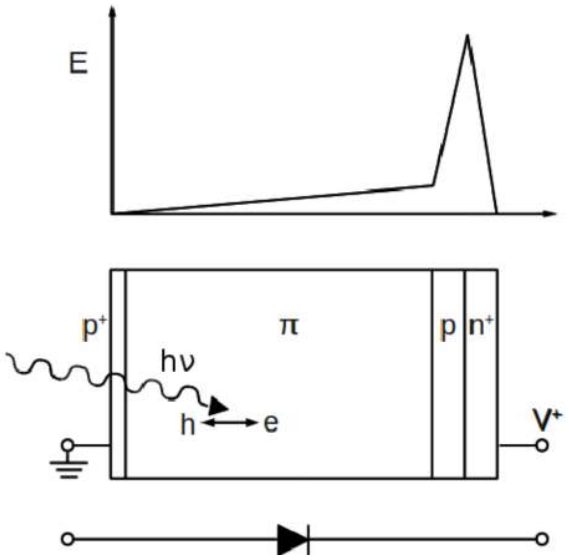


Figure 1.6: Schematic view of an APD, which is reversely biased and driven in reach-through mode. The figure is taken from [30].

in general changes with temperature around 1-2 %/°C [3, 35]. A constant gain is mandatory for a stable operation and therefore both temperature and bias voltage have to be controlled. Increasing the gain (e.g. 1000 V) is possible but with the drawback of much higher noise and a higher gain variation. Because of the low gain of an APD, low-noise amplifiers are needed. Usually low-noise charge sensitive preamplifiers are used for PET-detectors, which show an integrating behavior. Thus, the time resolution of APDs is worse compared to PMTs, due to the slow amplifiers and the relatively low gain. Although they have a low gain, the $\frac{\Delta E}{E}$ is around 12 % for 511 keV with a standard PET-scintillator coupled to an APD, and therefore $\frac{\Delta E}{E}$ is comparable with PMTs for PET application. Nevertheless, APDs have a much higher QE of typically 60-80 %[X] and are insensitive to magnetic fields compared to PMTs.

By applying a higher bias voltage to the APD, the electrical field is strong enough so that both, e^- and holes will trigger an avalanche in the depleted region. The APD is now operating in breakdown or Geiger-mode. However, the continuously avalanching APD will result in high current and finally get damaged. Adding a quenching mechanism stops the avalanche with a voltage drop and prevents the APD from destruction. The avalanche breakdown achieves a gain of around 10^6. This

[X] Note that the QE and PDE for APDs are identical.

APD can only detect one photon and afterwards it has a short recovery time until it functions again. Thus, such an APD creates only binary signals and therefore the information about the amount of photons that hit the APD is not available anymore. The signal output is not necessary linear with the amount of detected photons. Assembling these APDs in a huge array of micro cells in parallel led to a new photodetector type which is explained in section 1.8.3.

1.8.3 Silicon Photomultiplier (SiPM)

An array of micro APD cells ($10 \times 10 - 100 \times 100\,\mu\mathrm{m}^2$) reversely biased above breakdown is called SiPM. It is typically distributed in an active area of $1 - 3\,\mathrm{mm}^2$. It is also called *Micro-pixel Avalanche Photodiode* (MAPD), *Geiger Mode Avalanche Photodiode* (G-APD), *Multi-Pixel Photon Counter* (MPPC) or *Solid State Photo Multiplier* (SSPM). The applied electric field reaches gains up to 10^6. In contrast to an APD, not only the e^- but also in the holes contribute in the avalanche process of the SiPM. The fast travel speeds of the involved electrons and holes and the short travel distances result in an excellent *Single Photoelectron Time Resolution* (SPTR) for SiPMs. As mentioned in section 1.8.2 a quenching resistor is required inside the SiPM to stop the permanent avalanche process. Thus, independent of the amount of incident photons, every avalanche process results in a similar analog signal followed by "dead time" or "recovery time". The cell capacitance (C) and the quenching resistor (R) define the dead time (τ) with $\tau \propto \mathrm{RC}$.

The photon number information is lost when looking at a single cell but can be reconstructed when considering all micro cells of a SiPM. The SiPM output is therefore the sum of the triggered cells. Obviously, a SiPM has a maximal value which is the total number of micro cells. On the other hand, single photon detection becomes available because of the high gain and the short signal output width.

Between the micro cells, space is necessary to place the electronics. It also improves optical separation and has a positive impact on the electronic crosstalk. Although the QE of this devices is high, the mentioned geometric loss lowers the

sensitive area, which is expressed with the PDE for SiPM as[30]:

$$\mathrm{PDE_{SiPM}} = \mathrm{QE}(\lambda) \cdot \varepsilon \cdot \mathrm{P_{geiger}}, \tag{1.22}$$

where ε is the geometric fill factor (sensitive area), and $\mathrm{P_{geiger}}$ is the probability that an involved photon triggers a breakdown.

Increasing the micro cell size increases ε. Thus, a large micro cell size, like a $100\,\mu$m on a $1\,\mathrm{mm}^2$ SiPM device means a high PDE, but a low dynamic range since there are only 100 micro cells available. Because of the limited number of micro cells in combination with its dead time, the SiPM shows a non-linearly behavior and has to be calibrated with known photon fluxes. Thus, size and number of micro cells should be adjusted for every PET-detector. In that case, $\frac{\Delta E}{E}$ of an SiPM will become superior to that of a PMT because there is very little gain variation among the cells, the PDE is higher and the noise is negligible at room temperature [46].

Assuming an infinite recovery time for the micro cells, the number of fired cells ($\mathrm{N_{fired}}$) during a scintillation process can be calculated from the total number of micro cells ($\mathrm{N_{total}}$), the wavelength dependent PDE and its dedicated number of emitted photons ($\mathrm{N_\lambda}$) as follows[30]:

$$\mathrm{N_{fired}} = \mathrm{N_{total}} \cdot \left(1 - exp^{\frac{-\mathrm{PDE}(\lambda)\cdot \mathrm{N_\lambda}}{\mathrm{N_{total}}}}\right). \tag{1.23}$$

One problem of SiPMs is the after-pulsing probability caused by trapped carriers. It results in false pulses with fixed delays after the initial event appeared. Additionally, optical crosstalk of neighboring cells is observed in SiPMs. Optical crosstalk, dark count rate and after-pulsing will increase with increasing gain. The gain of SiPM depends on the bias voltage and temperature. However, relative to the supply voltage, SiPMs are more sensitive to temperature than APDs. The gain of a single cell is determined by the reverse bias voltage ($\mathrm{V_{bias}}$) above the overvoltage or breakdown voltage ($\mathrm{V_{break}}$) and the cell capacitance (C) with the elementary charge (e) as[30]:

$$\mathrm{gain} = (\mathrm{V_{bias}} - \mathrm{V_{break}}) \cdot \mathrm{C}/e \quad . \tag{1.24}$$

V_{break} varies with temperature on the order of 40 mV/°C [44, 45]. Therefore V_{bias} and the temperature need to be controlled for reliable results. Since P_{geiger} increases with gain, the PDE will increase with gain. However, V_{break} cannot be set to infinite values (usually 1-5 V greater than V_{bias}), since the SiPM functionality will be interfered by spontaneous breakdowns initialized by increased dark count rate and high after-pulsing probability. Although SiPMs have high gains, additional amplifiers are mandatory to trigger on the first scintillation-photons in PET-applications.

The logical next generation of an SiPM is already in development and called the *Digital SiPM* (dSiPM). One of the first approaches of dSiPM is the *Philips Digital Photon Counting* (PDPC) [60]. Every micro cell of this device can be read out digitally with a computer and provides the time information when it is triggered. This means, that the complete readout electronics is integrated onto the sensor and the analog part has almost been eliminated. Electronics noise plays a minor role, since the output of the dSiPM does not depend on the gain of an individual micro cell. To date, the environmental temperature has to be low for satisfactory results [60]. The dSiPM has a lot of potential and will be of interest when available for relatively low cost and the main issues are resolved.

1.9 Analog Signal Processing (Readout Electronics)

To process an analog signal is basically measuring and analyzing voltage changes over time, like e.g. the electric charge coming from a photodetector. In order to analyze these signals, several signal-acquisition-devices (readout electronics) are available and will be introduced in the following six sub-sections. Whereby, the focus lies on the reliability of computing the correct arrival time of the incoming analog signals. A detailed description of all boards that are used in this work, and utilize the following signal-acquisition-concepts, can be found in section 2.4.

1.9.1 Leading-Edge Discriminator (LED)

A *Leading-Edge Discriminator* (LED) is basically a comparator (differential amplifier) with an adjustable *Threshold* (TH) [61]. Thus, an LED does not respond to

input pulses below a certain TH level. If the input pulse height exceeds a given TH, a signal output is produced. At the input, the LED has to deal with pulses that vary in shape and amplitude. Additionally they arrive randomly in time. The standardized output signal is connected in time to the leading-edge crossing of the TH. The height of the output signal is constant and only depends on the used logic standard (like NIM or TTL). The width of the output pulse is variable and can be adjusted according to the measurements. The output signal comes with a constant delay which must be calibrated to get the true time information. Additionally, the output signal comes with an error, which is known as the walk effect and basically caused by the input signal varying its shape. This error can be reduced to a minimum by using a *Constant-Fraction Discriminator* (CFD) which is explained in the following section 1.9.2.

1.9.2 Constant-Fraction Discriminator (CFD)

Electronic signal pulses of photodetectors often vary in their amplitude, but are constant in reaching this plateau. Thus, it makes sense to compute the time always at the same fraction of the leading edge of the pulse. This is accomplished by a CFD. The CFD splits the signal into three parts. One part is fed through a comparator with an adjustable TH. The TH should be tuned according to baseline noise rejection or favored pulse heights. So, the first part of a CFD is just a simple LED. The two other parts go to an inverting and a non-inverting input of a second comparator one part of which is delayed and the other part is attenuated by a given fraction. Both comparator outputs are then fed through an AND-gate that now produces a walk-corrected output signal. The delay and the fraction depend on the signal. An example is given in fig. 1.7. In order to get the time point where 20 % of the amplitude (A) is reached of the signals leading edge, one would chose a fraction (f) of 20 %. Additionally one would have to calculate the delay (t_A) in dependence to the rise time (t_r) of the signal, as:

$$t_A = t_r \times (1 - f) \tag{1.25}$$

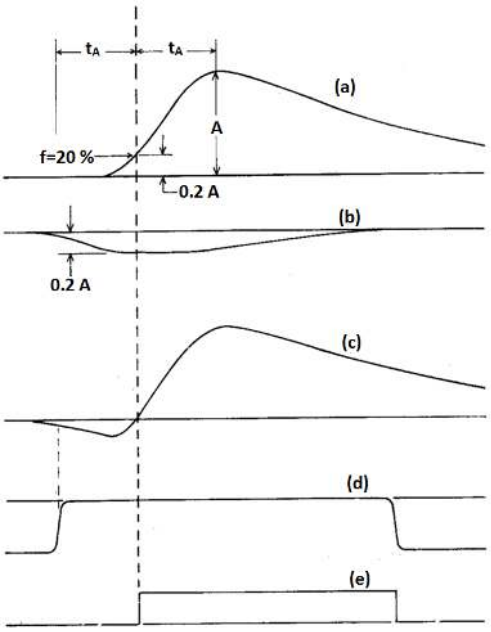


Figure 1.7: One can see an example signal pulse (a), which is delayed by t_A. The original pulse is attenuated by f (b). Both signals form a zero-crossing pulse (c) produced by a comparator. The zero-crossing, which is symbolized by a dashed line, is inside the given gate (d) that is provided by a second comparator with an adjustable TH ($f \times A$). An AND-gate (e) finally produces the standardized CFD output signal. The figure is adopted from [62].

If the rise time of the signal would be 10 ns, one would delay the signal by $t_A = 8\,ns$. Thus, t_A is the time between the point of interest and the amplitude of the signal. The delay t_A is typically done by externally adding one delay-cable before the second comparator input [62, 63] and has to be optimized according to the experiment. Every CFD-module usually provides a monitor output, where the zero-crossing point can be checked and adjusted with a screwdriver which basically changes the electric resistance of the walk compensation network. To optimize the walk compensation network one has to trigger on the CFD-output and display the monitor output on an oscilloscope screen. If the monitor pulse is stable in time, the optimal setting for cable delay and fraction (screwdriver) is accomplished [64].

1.9.3 Time-to-Digital-Converter (TDC)

A *Time-to-Digital Converter* (TDC) consists of a comparator with an adjustable TH. It is driven by a fast periodic clock in the *Gigahertz* (GHz) range and is comparable

to a very fast working LED. But with the disadvantage that the output signal time depends on the clock. This limits the resolution to the clock period. Additionally the walk effect is a problem as mentioned in section LED. That's why typically the signal is fed through a CFD before it goes to the TDC. In practice (e.g. for PET) a "multistop" TDC is used that has several channels in parallel. They are all triggered by a global start trigger. Each of the channels are connected to independent stop triggers (e.g. CFDs), which allows time resolution measurements for many events in parallel [3]. TDCs can have a time resolution in the ps-region for coincidence measurements up to a *Millisecond* (ms) [65].

1.9.4 Analog-to-Digital Converter (ADC)

The digital output of an *Analog-to-Digital Converter* (ADC) is proportional to an analog voltage, supplied to the ADC-input. A perfectly behaving ADC is linear. In reality the error of the nonlinearity is described by the *Differential Nonlinearity* (DNL) and can be calibrated out to a certain extend. Every ADC comes with a resolution or bit-depth. E.g. an 8-bit ADC will produce $2^8 = 256$ discrete states. This is a resolution of $\frac{1}{256}$ or less than 0.4%. The final decision of which ADC is needed for an experiment is limited by the SNR. If the SNR is 0.5 %, an 8-bit ADC would be the right choice. Additionally, an ADC runs with a certain speed measured in samples per second. A sampling speed of 1 *Gigasamples per Second* (GSPS) would provide in the upper case an additional number between 1 and 256 for every sampling interval (1 ns). The fastest ADC-type is the flash ADC. It basically consists of 2^n comparators, where n is the bit-depth. The input voltage is split in this case to 256 inputs. An additional logic is connected to the comparator outputs and produces the numbers. The many electronic components causes the fast ADCs to consume a lot of power. More details about ADCs can be found in specialized literature like the book from Knoll [3].

1.9.5 Time-to-Amplitude Converter (TAC)

A *Time-to-Amplitude Converter* (TAC) is a device that produces an output signal, whose amplitude is proportional to a measured time. The time is measured between two input signals that are usually labeled START and STOP. Both inputs are standardized (e.g. NIM logic). First a START signal has to arrive. It triggers

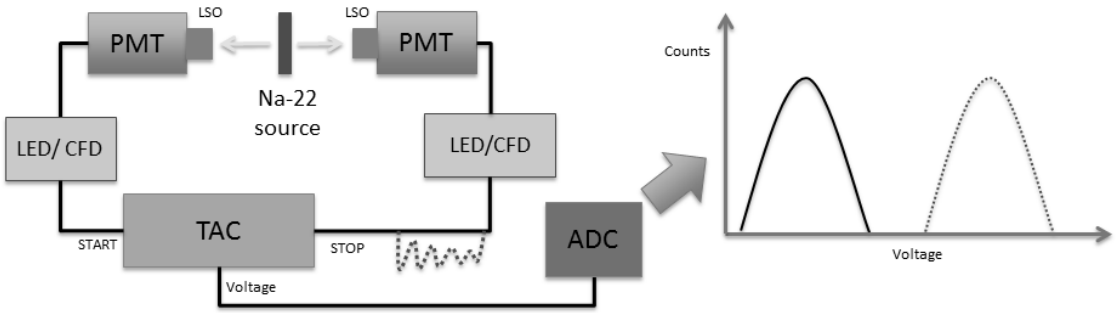


Figure 1.8: It shows a test setup for a PET-measurement. One can see that many modules are required to measure time resolution with a TAC. Two measurements with varying cable delay, represented by the two distributions, are required to obtain the time resolution. The dashed zigzag line stands for the other cable delay.

a capacitor which begins changing linearly until it gets stopped by a STOP signal arrival. One has to guarantee that the STOP always arrives at a given delay compared to the START. The voltage of the capacitor can now be measured with a voltmeter. However, since multiple measurements are performed, the TAC-output is typically fed through an ADC with a high resolution. So far only one normal distribution of voltages is measured. In order to receive proper time information, an additional measurement has to be performed with an increased cable delay for the STOP. The enlargement of the cable delay must be known and will be proportional to the mean voltage increase of the TAC output. One meter of a common coaxial cable would approximately shift the Gaussian-distribution by 5 ns in time, which corresponds to a measured mean voltage shift. However, there are several error factors that add together [3]. The TAC automatically consists of the errors that come with the START and STOP signals. Usually an LED or a CFD produces such a signal. Additionally the TAC has errors, like the non-linearity of the capacitor and the noise. Finally the ADC adds an error mainly caused by its bit-resolution. A

test setup for a PET-measurement using a TAC is illustrated in fig. 1.8.

1.9.6 Switched-Capacitor Array (SCA)

An SCA is an *Application-Specific Integrated Circuit* (ASIC) which provides analog signal recording at high sampling speeds. To a certain extend an SCA is comparable to a very fast ADC. An SCA requires less power than a high speed ADC and, more importantly, is available at lower cost. One of the first fields of application is the particle detector readout which started in the 1980's as shown by Kleinfelder et al [66].

The idea behind these chips is to continuously sample at a high rate (e.g. 1 GSPS) and to store the data for a short period of time in the SCA, which will be overwritten again and again. After a trigger, the sampling in the SCA stops and the analog information (e.g. a PET-detector) can be read out with a slow ADC, e.g. 33 *Megahertz* (MHz). This data speed is now acceptable for evaluating in real time before storing the important information onto a hard drive or simply displaying the signal on the monitor screen, similar to an oscilloscope. Hence, one can enhance the sampling speed of a slow ADC with an SCA. An illustration is given in fig. 1.9 where each SP is artificially digitized 30 times faster compared to its digitization speed.

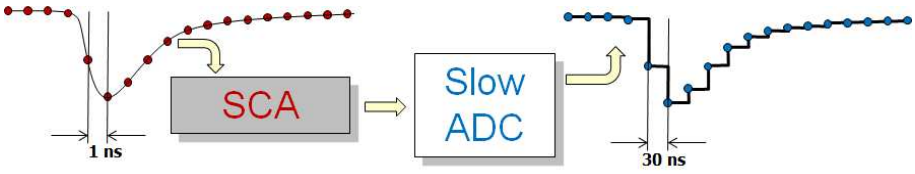


Figure 1.9: The SCA stores 18 information of an analog pulse with a speed of 1 GHz. Although the ADC is running at a frequency of 33 MHz, 18 SPs of the pulse are digitized in 1 ns steps.

The technical realization of an SCA is basically an array of capacitors running in a sample-and-hold mode. A fast sequence of write pulses allows the recording of analog waveforms in these capacitors. They can later be read out and digitized at a lower speed. First sampling speeds in the GHz region are demonstrated by Haller et al[67] utilizing inverter chains. Therefore, most modern SCAs use a kind

of inverter chain as delay lines to generate the write pulses which in turn open analog switches. Fig. 1.10 shows a simplified schematic of an SCA. To be accu-

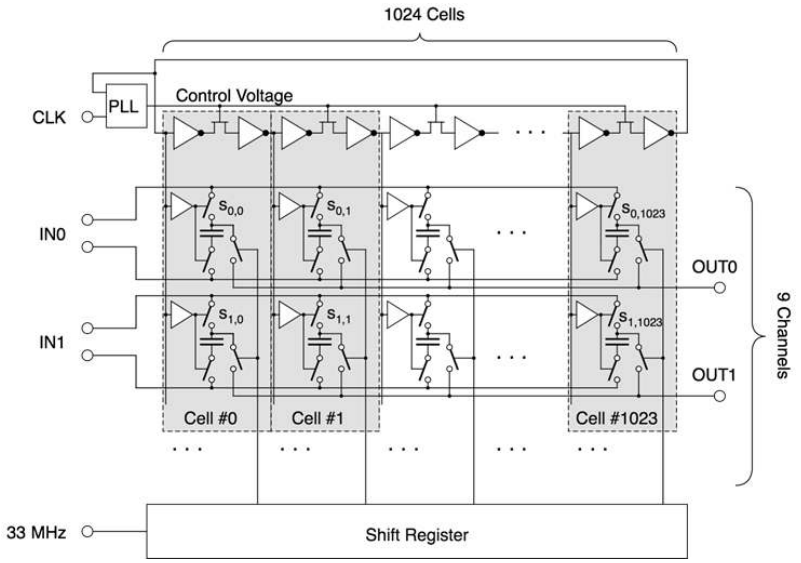


Figure 1.10: Simplified schematic of the DRS4-chip. One can see that is consists of 9 channels with 1024 cells each. All cells are controlled simultaneously by the same inverter chain. The figure is from Stricker-Shaver et al [31]

rate, it shows the DRS4, which is the fourth version of SCAs developed at *Paul Scherrer Institute, Switzerland* (PSI) [68]. The transition time of an inverter depends on parameters like temperature and supply voltage. To address this problem, most SCAs use an external constant reference clock together with a *Phase-Locked Loop* (PLL) or a *Delay-Locked Loop* (DLL) to stabilize the sampling frequency. Furthermore, mismatches between transistors in the CMOS process cause each inverter to have different transition times. The effect comes from the geometrical size of the transistor and the doping properties. It is stable in time and therefore it can be calibrated by measuring the true transition time of each inverter. This measurement and its correction is one of the main topics of this work. The theory of several new calibration techniques for SCAs can be found in chapter 2. SCAs commonly use CMOS technology. The maximum sampling speed has increased over the years. Current SCA-chip versions from different groups allow sampling speeds in the range of $0.1 - 25\,\mathrm{GSPS}$ [69–71]. They have SNRs equivalent to $8 - 13\,\mathrm{bits}$ with sampling depths of $256 - 64000\,\mathrm{cells}$ per channel. Their typical power consumption is around 10 *Milliwatt* (mW) per channel. Thus, these chips are excellent alternatives for com-

mercial flash ADCs, where the power consumption can become several Watts per channel for sampling speeds in the GHz region [3]. On the other hand, all SCAs share the drawback that the time required to read out the capacitor cells causes dead time. It depends on the number of channels and storage cells. The dead time is typically in the range of 0.3-100 μs, which limits the application to cases where the trigger rate is low. A trigger rate of 100-1000/s is a relatively easy task for an SCA readout solution. However, even for this trigger rate events will be lost. The optimal application for SCAs therefore lies in fields with low trigger rates, excellent time resolution, pile-up rejection and the requirement of many synchronized readout channels. This includes for example particle physics [72], Cherenkov telescopes in gamma-ray astronomy [73], TOF applications [74] and neutrino physics [75]. Also, in medical imaging, specifically in PET, where TOF is of interest [28], SCAs are candidates for upcoming applications. Schaart et al [29] measured for PET signals a CRT of 100 ps (FWHM), where the fast scintillator $LaBr_3$ was utilized. In other words, the time resolution of a single PET-detector is around 30 ps (σ). This indicates that the readout electronics of this PET-detector must have been very precise.

An SCA-based readout electronics of micro channel plates measured a single channel resolution of around 15 ps (σ). This result is comparable with the best commercial combination of a CFD with a TAC, but at a lower cost per channel[76]. Another SCA-based readout electronics utilizing the DRS4-chip gave convincing results with time measurements of straw tubes [77], although the accuracy was limited by the imperfect TC-method, but this was the only available TC-method at that time. Therefore, one focus in this thesis is finding the best TC-method for the SCA technology by utilizing the DRS4-chip.

1.10 PET-Detector and Block-Detector

The energies of PET-events are too high to be directly detected by common photodetectors. Therefore a scintillator is used to stop the γ-ray, resulting in a predicable amount of photons for a given energy. These isotropically emitted scintillation-

photons travel inside the ideally transparent crystal and get partially absorbed or get reflected at the crystal walls until they arrive at the photodetector. There are several factors influencing the amount of photons that will be detected at the photodetector side. For example, one can wrap a crystal with white *Polytetrafluoroethylene* (PTFE) tape[XI] causing light reflectance $> 99\%$ at the relevant five crystal surfaces [78].

Also the optical bonding between the photodetector surface and the scintillator is of importance. The n of the bonding material ($n_{bonding}$) should ideally be $\sqrt{n_{detector} \cdot n_{scintillator}}$. If both indices of refraction are identical (but $n \neq 1$), one still needs a dedicated bonding material to prevent light loss caused by the connecting air gap. In common PET-scanners generally around 20 % of the scintillation-photons of absorbed 511 keV events are finally detected and converted to an electric signal [79].

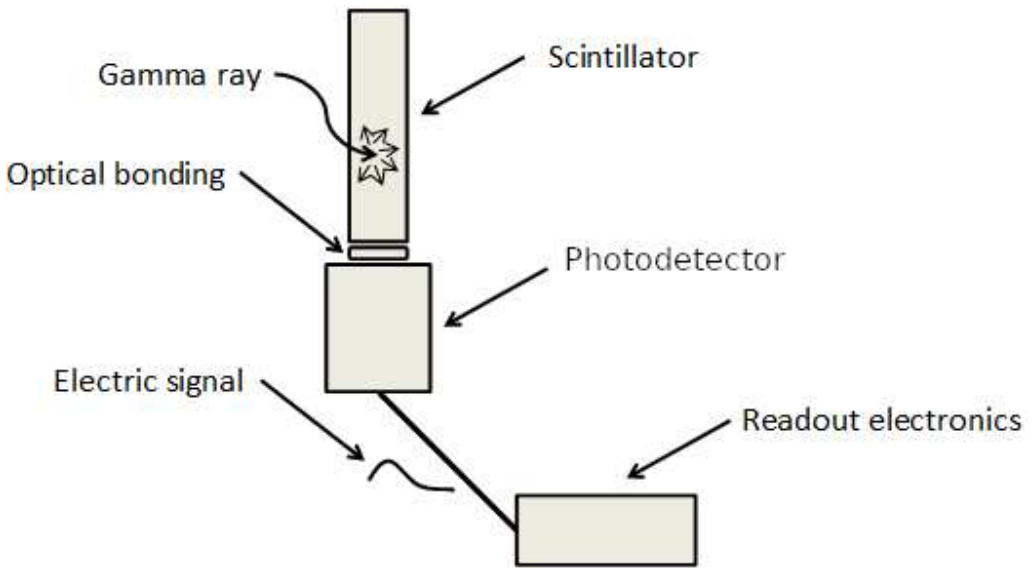


Figure 1.11: Schematic view of a scintillator coupled to a photodetector.

In fig. 1.11, a PET-event is illustrated for a single crystal coupled to a photodetector (also called: one-to-one coupling). The minimum requirement to acquire a PET-image are two facing one-to-one coupled, rotatable PET-detectors, as proven by the first published PET-image of a human brain [80]. However, it makes sense to surround the object of interest with many facing PET-detector pairs, as illustrated

[XI] PTFE tape is commonly also called teflon tape or seal tape.

in fig. 1.1(a), to increase the detection sensitivity of the scanner. As a result, one will have a high number of photodetectors, scintillators and readout channels. To reduce cost for readout channels, a so-called Anger-logic is used basically in every PET-scanner [81, 82]. The idea of Anger-logic is to lower the number of readout

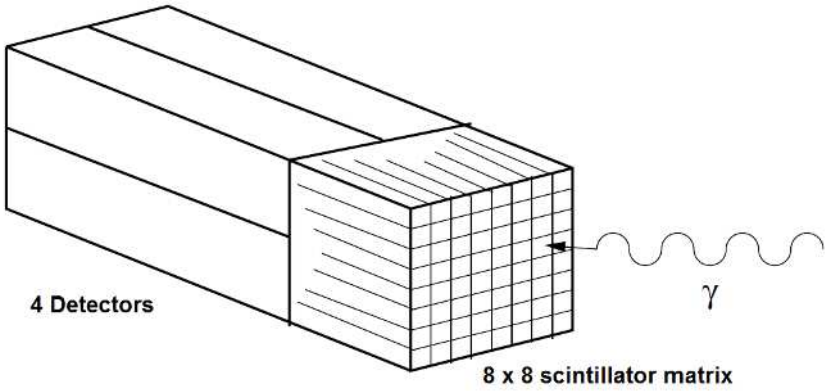
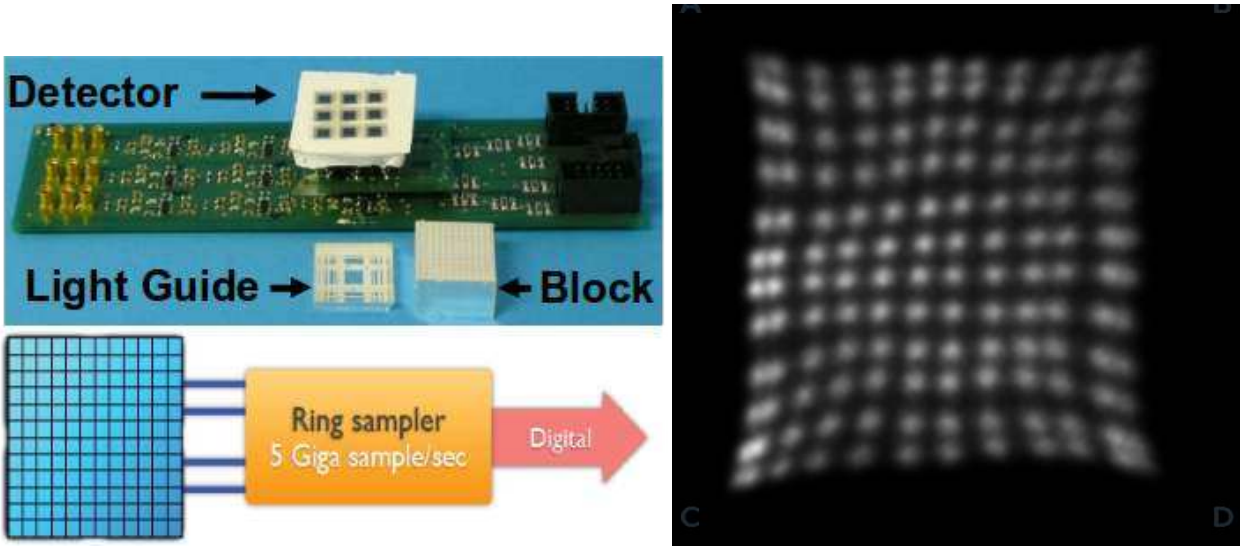


Figure 1.12: Schematic view of a detector-block consisting of 4 photodetectors coupled to a 8×8 scintillator matrix. The figure is taken from [2].

channels by weighting the light spread in a pixelated scintillator-block with a minimum amount of output channels. Thus, the detector-block in fig. 1.12 reduces the number of readout channels from 64 sequential scintillation crystals to 4 photodetectors. If a PET-event hits a single crystal in the scintillator-block, each of the four photodetectors will measure a fraction of the produced scintillation-photons. This way the interacting crystal of a detector-block can be reproduced.

Additionally, a light guide (few mm) can be placed between the photodetectors and the scintillator-block to guarantee that the photons can spread to the correct area. The use of a light guide is an elegant solution to recover every crystal location in the flood histogram (also called: position profile or crystal-map) of densely packed crystal arrays. In fig. 1.13 one can see such a flood histogram digitized with 4 channels of the DRS4-chip. The 3×3 photodetector channels had to be multiplexed to 4 channels in order to apply the Anger-logic.

Note: A one-to-one coupling will always provide the best CRT, because the maximum amount of photons are detectable, with best results around 120 ps (FWHM) [83] when coupled to LSO. In contrast advanced TOF-PET systems utilizing detector-blocks have a CRT of around 500 ps (FWHM)[28].



(a) Detector-block **(b)** Flood histogram

Figure 1.13: It shows a detector-block consisting of a 3×3 photodetector array, a light guide and an 12×12 crystal block (a) and the resulting Na-22 flood histogram (b) sampled with the DRS4 running at 5 GSPS. The upper picture in (a) is adopted from [79].

1.11 Motivation of this Work

Detectors in large high energy physics experiments or medical imaging applications which detect radioactive particles are usually used to measure parameters like Γ, the exact energy of the particle or its accurate moment of interaction. The uncertainty of measuring the correct moment is usually expressed by the term "time resolution". A detailed derivation for time resolution can be found in section 1.6. In short, it stands for the error in time of a single measurement and is commonly described by the quantity "σ" or "FWHM" (FWHM $\approx 2.4\sigma$).

Specifically in coincidence detectors such as Compton cameras [3], calorimeters in high energy physics experiments [84] or in medical imaging systems like in PET, the exact determination of the photon arrival moment at the detection is required. For PET the arrival times of two simultaneous photons that result from annihilation is permanently measured ideally with a time resolution of several ps. This enables coincidence timing providing the exact spatial determination of the interaction location or annihilation location.

The time resolution in PET systems depends on the electronic noise and the speed of the readout electronics as well as the measurement errors of the individual parts of the PET-detector. Because of the quadratic contribution of the individual errors as described in (1.14), one should ideally always reduce the error that has the biggest impact on the overall error. In order to calculate one individual error, one has to measure all the other errors. Equivalent to this approach is to reduce an error so much, that is has no measurable effect on the overall error.

Measuring and improving the time resolution in nuclear imaging applications is a major topic of this work. On this note the focus of this work is to optimize a readout electronics to measure in the ps-region. Besides using real coincidence PET signals to evaluate a readout electronics, which is also done in this work, it is more convenient to measure the time resolution between two signals coming from a function generator. This approach minimizes the previously described errors of the input signals providing only the time resolution of the utilized readout electronics. The state of the art readout electronics for PET systems is a combination of TDCs for the timing information and slow ADCs for the energy information. With this approach our preclinical PET-INSERT that is also investigated in this work results in a CRT of around 4 ns (FWHM). Due to its short LOR, a preclinical-PET would require a CRT below 100 ps (FWHM) to be called TOF-system. This cannot be achieved with the TDC used in the PET-INSERT which on its own has an error bigger than 333 ps (σ). Thus, the readout electronics error for small animal applications should ideally be below 10 ps (FWHM). Due to (1.14) such a readout electronics has no measurable effect on the overall CRT to the TOF-preclinical-PET ($\sqrt{100^2 + 10^2} < 101$). A promising candidate from the SCA technology is investigated which is the DRS4 [XII]. It provides sampling information like coming from a fast ADC. Several fast ADC measurements in this work prove that a time resolution below 10 ps can be achieved.

Using an SCA as readout electronics has several advantages compared to a fast ADC such as low power consumption, low cost per channel, better bit-resolution and faster sampling speed. On the other hand, the time it takes to read out an SCA causes dead time. The dead time is the biggest drawback for the usability

[XII] A more detailed description of SCAs can be found in section 1.9.6.

in PET applications, where millions of events per second are analyzed in real-time and ideally no event should get lost. Additionally, the utilized SCA, the DRS4, performed worse compared to a slower and inferior ADC. All the problems that came up with earlier experiments when measuring with the DRS4 are understood and will be explained in detail [XIII].

One goal of this work is to identify the best time resolution that is theoretically achievable with a DRS4-chip. Thus, this work is not only limited to PET applications. Improved σ for time measurements and fast sampling speed will become important in other fields such as TOF mass spectrometry[85], *Light Detection and Ranging* (LIDAR)[86], high energy physics experiments[87], etc.

Ultimately the author will address the issue of the technological direction of PET towards TOF. Therefore, one major question that is answered in this work is whether the SCA technology is of interest for PET.

[XIII] A full spectrum of the initial DRS4 problems can be found in the first two sections of chapter 3.

Chapter 2

Material and Methods

At the beginning of this chapter which is grouped in 5 sections, several digital signal processing techniques are pointed out in terms of their usability for PET. Specific digitizing devices, the SCA-based boards, are familiarized in detail to various new calibration methods. The DRS4-chip is exclusively investigated as an SCA representative. The terminology SCA is kept to emphasize that the developed methods can be applied to all SCAs including the DRS4. Therefore, an abbreviation containing the terminology "SCA" in an experiment always refers to the DRS4-chip! Further, other utilized hardware of this work is introduced and abbreviations are given to these devices. At the end of this chapter the basics for all performance tests with respect to time resolution measurements are provided.

2.1 Digital Signal Processing Techniques

Traditionally, for PET modality when using photodetectors, the interface between the photodetector and the front end electronics has been an analog signal chain. This is also the case for the investigated PET-INSERT. The photodetector signal is split to separate time and energy measurements. The energy signal goes through some form of pre-amplification and then to an ADC in order to process the energy information. Meanwhile, the time signal goes through a CFD and then to a TDC.

If the circuit is to be made completely digital at the detector front-end electronics, only a few ways are presently available to accomplish this efficiently. Work in the

research community has shown that the *Field-Programmable Gate Array* (FPGA) reached a point in its development, where it can be used as a replacement for the time elements (CFD and TDC).

One way of realizing a digital solution for PET signal processing is to begin with a low-noise amplifier, running the signal into an ADC and then into the FPGA. Brute force methods have been demonstrated utilizing high end flash ADCs beyond 1 GSPS and FPGA-based TDCs towards 5 ps resolution, but they require a lot of power and are expensive to implement[88–91]. Thus, SCAs are also candidates for future applications acting as ADC replacements, if the dead time problem is in an acceptable range.

Against this background the following digital analyzing techniques are dissected and further developed. It should be mentioned that a core theme is straightforwardness in the following processing techniques, making them applicable to FPGAs. These techniques are rewind in the following five sub-sections.

2.1.1 Digital Leading-Edge Discriminator and Fitting

The digital LED can be derived directly from the analog LED as described in section 1.9.1, where a given TH will result in a time point when this TH is reached. Since the dataset consists out of many SPs, the most common approach is the interpolation between the two SPs of the leading edge surrounding the TH level (2-points LED). In order to obtain the time information always at the correct TH level, the waveform is first corrected to the baseline offset. This is accomplished by averaging some SPs of the baseline and then subtracting this average from all SPs. In fig. 2.1 such a 2-points LED is illustrated, where the red dot symbolizes the moment of the TH crossing. The time resolution of a digital LED is predictable as described in section 1.6.2 and will improve by using more SPs. Three fitting methods - the linear, the parabola and the spline fit - are applied alternatively to the 2-points interpolation to operate a digital LED. More details about fitting, spline-approximation, digital filters and digital data processing in general can be found in a book from Schrüfer[92] and Knoll [3].

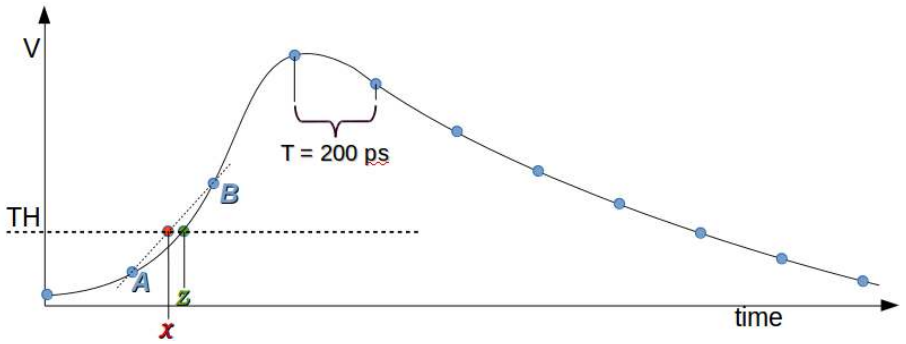


Figure 2.1: Drawing of a 2-points linear interpolation which is the simplest way of running the digital LED. One can see an analog pulse symbolized by a black line and an example of a possible equidistant digitization (5 GSPS, blue circles). A and B stand for two possible SPs below and above the TH. x is the linear interpolated (wrong) time point. Whereas, z symbols the correct time point. The walk error between x and z changes with the signal shape.

2.1.2 Digital Constant-Fraction Discriminator

There are several ways of realizing a digital CFD. Probably the most common one can be directly copied from an analog CFD (section 1.9.2). Since the input signal is digitized one can easily split, invert or attenuate the SPs as an analog CFD. Considering that the purpose of a CFD is to prevent the walk effect (fig. 2.1), one can also normalize the waveform and afterwards perform the digital LED. Thus, any digital LED where the walk effect is calibrated out, can be understood as a digital CFD.

2.1.3 Zero Adding with Low-Pass Filter

This method is similar to the spline-approximation. Thus, it can be used to generate additional SPs in a waveform. The basic idea is to add equidistant SPs between known SPs, which are initialized with 0 mV (zero adding). After convoluting the changed waveform with the *sinc*-function:

$$sinc(t) = \frac{sin(at)}{at}, \tag{2.1}$$

a new waveform will result where the added 0 mV points will have an interpolated value. By changing the filter parameters a one can tune the new shape of the wave-

form. Additionally the noise level will be reduced, which can lead to an improved result with regards to time resolution and energy resolution. An example is given in fig. 2.2 where a *Sampling Speed of the SCA* (f_{SCA}) of 2 GSPS is artificially increased by a factor of 10, resulting in 50 ps sampling steps.

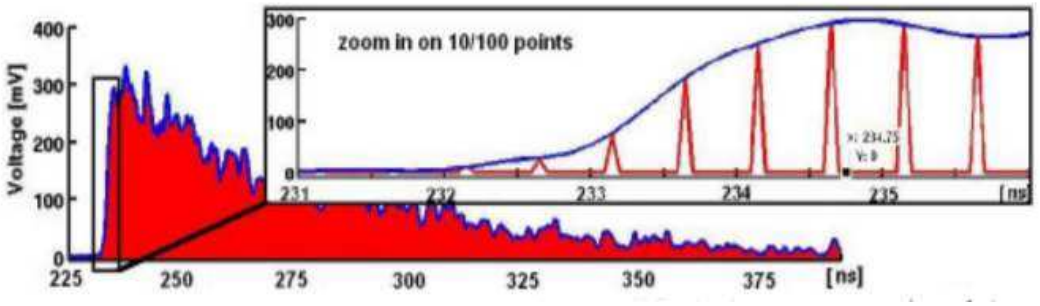


Figure 2.2: Interpolation via convolution of a modified photo-sensor-signal (zero adding) and the sinc-function. The red line is the signal waveform, the blue one its interpolation. The upper plot is the zoom in on the rising edge. The top of every triangle stands for a truly sampled point. 9 additional SPs lie between two triangles. Each of the two sets of points is connected by a line for clearness.

2.1.4 Cross-Correlation

Cross-Correlation (CC) basically provides the similarity between two functions as[92]:

$$\mathrm{CC}(\tau) \;= \int_{-\infty}^{\infty} f^*(t) \cdot g(t+\tau)\, dt \;, \tag{2.2}$$

where $\mathrm{CC}(\tau)$ results in all positions of f relative to g and f^* stands for the complex conjugate of f. For a discrete waveforms as coming from an ADC, CC can be defined as[92]:

$$\mathrm{CC}[n] \;= \sum_{m=-\infty}^{\infty} f[m] \cdot g[m+n] \;. \tag{2.3}$$

$\mathrm{CC}[n]$ provides a value for waveform g shifted over waveform f from the left to the right. $\mathrm{CC}[n]$ will result in the biggest value if both waveforms are overlapping best. For (2.3), equidistant SPs are mandatory, like it is the case for typical ADC outputs. The digitized SPs from the DRS4 are not equidistant. Instead the DRS4 curve is sampled with 1024 different sampling intervals and thus, it is not possible to

directly cross-correlate two DRS4 signals with each other, Therefore, two approaches are developed in this work to perform a cross-correlation with DRS4 data.

One approach will be referred to as *Interpolated Cross-Correlation* (ICC), where the SPs are made equidistant by computing the missing points (e.g. 500 ps steps) through linear interpolations of the adjacent digitized known points. An example could look as follows:

$$\begin{aligned} 1^{\text{st}}\text{ DRS4 sampling point:} \quad & (0\,\text{ps} \,|\, 100\,\text{mV}) \quad -> \quad (0\,\text{ps} \,|\, 100\,\text{mV}) \\ 2^{\text{nd}}\text{ DRS4 sampling point:} \quad & (513\,\text{ps} \,|\, 404\,\text{mV}) \quad -> \quad (500\,\text{ps} \,|\, 396\,\text{mV}) \\ 3^{\text{rd}}\text{ DRS4 sampling point:} \quad & (1056\,\text{ps} \,|\, 852\,\text{mV}) \quad -> \quad (1000\,\text{ps} \,|\, 806\,\text{mV}) \\ & \vdots \end{aligned} \tag{2.4}$$

Afterwards the resulting equidistant waveforms can be cross-correlated directly. This approach functions only for split pulses. In fig. 2.3 an cross-correlation example of two equidistant waveforms is illustrated. The ICC suffers from the *Linear Interpo-*

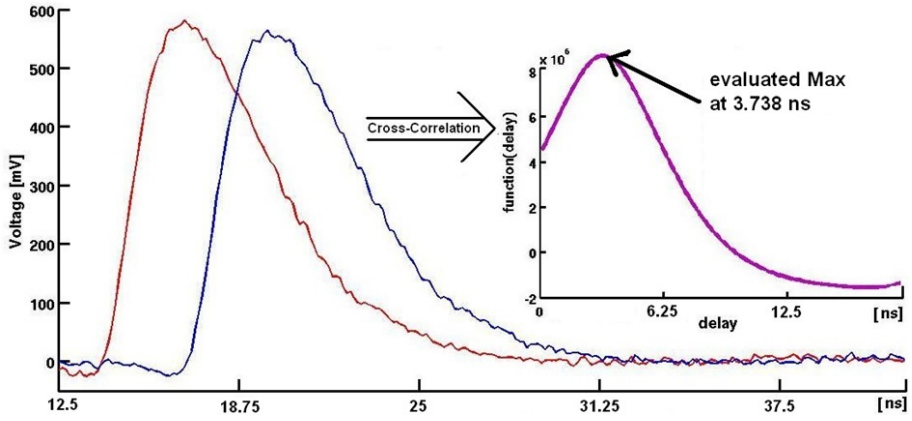
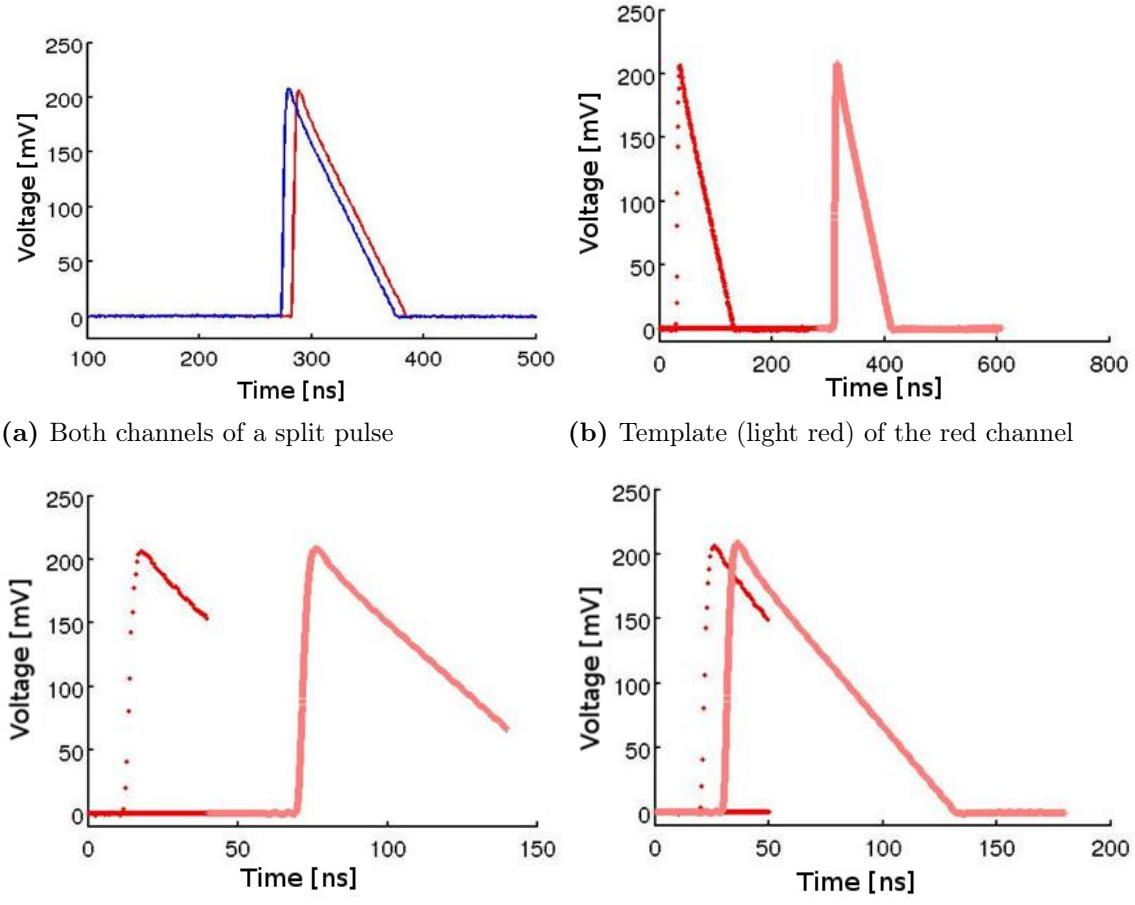


Figure 2.3: One can see a split pulse. The blue channels is approximately 4 ns delayed towards the red channel. The peak of the purple cross-correlation curve provides the exact delay of 3.738 ns.

lation Error (δ_{lin}) which is explained in section 2.2.8. The ICC is applied only once in this work. The results can be found in in section 3.3.3 and additionally in fig. 1.4.

A more exact approach was developed at the beginning of the thesis, where there was little experience with the cross-correlation method in combination with the DRS4. Consequently, this approach will be referred to as *Precise Cross-Correlation*

(PCC). PCC is rather extravagant and differs considerably from ICC. Since the PCC is more precise one would expect improved results for all ICC-evaluations if repeated with the PCC. An additional feature of the PCC is that it can be applied to calculate the time between signals that have different shapes. To achieve this, templates are needed for the PCC which have the same shape as the expected signals. To get a first understanding of the PCC one should notice that the sampling intervals from the DRS4 are provided in 1 ps accuracy. Therefore, a template with 1 ps steps is produced. Its maximum is placed at a known position as illustrated in fig. 2.4(b), where the maximum of the template is located at 350 ns. Afterwards the timing



(a) Both channels of a split pulse

(b) Template (light red) of the red channel

(c) Decreased amount of SPs

(d) Signal shifted towards template

Figure 2.4: The plot in (a) shows two channels of the DRS4 running at 2 GSPS. In (b) one can see the computed template of one channel located at 350 ns (right) and one modified signal where the unknown SPs are set to zero (left). (c) shows the same signal as (b) but with less information. In (d) one can see that the computed template is virtually shifted towards the signal.

is provided through the comparison between template and measured signal pulse.

This method works accurately and will be explained in the following lines in more detail.

When running the DRS4 at 2 GSPS, the sampling steps are in the 500 ps region and all unknown 1 ps-steps of the signals are set to zero [I] before applying the cross-correlation. Since the time difference (delay) between two signals is to be calculated, two templates must be computed, one for each channel. The two templates are only produced once, thus for a new delay, the old templates can be utilized again. To produce the templates two approaches are tested, the spline fitting and zero adding in combination with a lowpass filter. In both cases several thousand produced templates are averaged with the Levenberg-Marquardt algorithm. The results of both methods are identical and therefore the faster method, zero adding with lowpass filter, is utilized.

The example fig. 2.4(a) shows a split pulse measurement with a rise time of 4 ns. For better understanding in fig. 2.4(b) only one channel is displayed showing two similar looking waveforms. The waveform in the middle part is the calculated template for the PCC. On the left of this plot, one will find a single measurement of the split signal with zero adding. Since the signal on the left is not in its original shape (zero adding), it will further be referred to as the modified signal. This is also the case for fig. 2.4(c & d). Cross-correlating the two functions in fig. 2.4(b) will result in the time difference between template and modified signal.

To reduce computing time of the CC only the area of the modified signal that provides the best position information should be used. This is usually the rising edge of the modified signal. An example is illustrated when comparing fig. 2.4(b vs. c). In fig. 2.4(c) one can see that 40 ns of the original signal is further processed. To reduce computing time even more, the PCC consists of two steps per channel. First the time difference between template and modified signal is roughly calculated using a digital LED. Afterwards, the modified signal is virtually shifted around 10 ns next to the template (fig. 2.4(d)), which is around 20 SPs for 2 GSPS but 10,000 SPs in the template. In total, the modified signal consists of 40,000 1 ps-steps, but only 80 SPs have a value which is not zero (fig. 2.4(d), waveform on the left). On the

[I] This technique is called zero padding or zero adding.

other hand, the template consists of 180,000 computed SPs. Since the modified signal is virtually shifted next to the template, one would expect the biggest value of the cross-correlation function in the region of the $10{,}000^{\text{th}}$ iteration. The resulting cross-correlation function, which provides the time difference at its peak position, can be further improved, below the 1 ps steps, by a parabola fit of the peak.

Finally, both time differences between each modified signal and its corresponding templates need to be calculated through cross-correlation. Since the templates of the two compared channels are sitting at the same position in time, the real time difference between the two sampled signals is simply the difference between the two via cross-correlation calculated time differences. The time resolution for the provided example in fig. 2.3(a) when utilizing a digital LED results in 150 ps (FWHM) or 64 ps (σ). When applying the PCC instead, the time resolution improves to 30 ps (FWHM) or 13 ps (σ) which underlines its potential. The just introduced PCC is applied twice in this work. The results can be found in section 3.1 and section 3.2.

2.1.5 Reducing a Gaussian Distribution to 3 Values

Usually a Gaussian fit is performed if a measurement is very noisy or shows outliers. In general, this fit will result in a more accurate μ and σ. Under good conditions (like the distribution in fig. 1.4), it is much easier to calculate the μ using (1.10) and σ using (1.11). When calculating several thousand σ values at the same time, it is advantageous to use (1.12). As a result, a single distribution consisting of million of events (x_i) does not have to be saved anymore. Instead only 3 values will be overwritten every time a new x_i is measured for this distribution. These 3 values are the actual number of events i, the sum of all measured values x_i and the sum of all x_i^2.

However, outliers are not recognizable by this method and may result in wrong μ and σ. To reject outliers for this method, the following control algorithm is developed in this thesis:

σ is calculated after $i = 4$. If σ is too large, the 3 values are reset. If σ is acceptable, the 3 values are continuously modified by adding more events x_i. Thereby, all x_i with an error greater than $\mu \pm 3\sigma$ will be rejected. This algorithm reduced the

memory usage and computing time of the *Personal Computer* (PC) dramatically. But, it has to be adjusted according to the individual distributions.

2.2 Time Calibration (TC) Methods for SCAs

The sampling intervals of an SCA-chip are not equidistant, but constant over time. This means the SCA has to perform a TC before an accurate time measurement can be made. It is recommended to perform the TC after a VC is utilized, which is described in section 2.3. Temperature variations also change the result of the TC and should not be ignored (see section 3.3.1).

Several TC-methods for SCA-chips are available in the literature[71, 74, 93, 94]. For the DRS4 which is an SCA-chip, two TC-methods provided by PSI and *Costruzioni Apparecchiature Elettroniche Nucleari S.p.A.* (CAEN) are tested in this work. Both TC-methods showed insufficient results. Therefore, a NEW-TC was developed during this thesis which solved the mentioned issues. Additionally, the University of Tübingen filed an international patent application[95] containing the NEW-TC. Both TC-methods from PSI and CAEN including the NEW-TC with all adjustable options will be explained in detail in the following 10 sub-sections. Three NEW-TCs are presented in this work. Their variations and combinations are discussed in section 4.3. Looking at the basic nomenclatures in sub-section 2.2.1 is recommended before approaching the following TC-methods.

2.2.1 Basic Nomenclatures in Respect of SCAs and ADCs

The two terminologies "cell" and "SP" have the same meaning with respect to SCAs. Both terminologies can be used to address specific capacitors of one SCA-channel. Thus, the number of capacitors is equivalent to the *Number of SCA cells* (n_{SCA}). A capacitor stores electric charge which reflects the analog signal information at a given time point. The electric charge of SPs is digitized with an ADC resulting, after proper calibration, in sampled voltages of the input signal. The *Voltage Difference*

(ΔV_b) between two neighboring SPs is defined as

$$V_b - V_{b-1} = \Delta V_{b-1,b} \stackrel{!}{=} \Delta V_b \quad . \tag{2.5}$$

When using the same nomenclature for time as in (2.5), one will result in (2.6). Thus, the *Local Time Difference* (Δt_b) is defined[II] as

$$t_b - t_{b-1} = \Delta t_{b-1,b} \stackrel{!}{=} \Delta t_b \quad . \tag{2.6}$$

"Δt_b" is sometimes also called the "sampling interval" between the cells b and $(b-1)$. It should be mentioned that the terminology sampling interval is common for an ADC where the SPs are equidistant in time and therefore it can be a misleading expression for an SCA.

By applying (2.6), the *Global Time Difference* ($\Delta t_{a,b}$) can be calculated with

$$\Delta t_{a,b} = \sum_{i=a+1}^{b} \Delta t_i \quad . \tag{2.7}$$

A Δt_b can therefore always be seen as a special case of the $\Delta t_{a,b}$. Another special case is $\Delta t_{a,a}$. It stands for the time difference of cell $\#a$ to itself which naturally is 0 ps. An alternative interpretation is that $\Delta t_{a,a}$ stands for the *Elapsed Time for one SCA Rotation* (T_{SCA}) as

$$\Delta t_{a,a} = \sum_{i=1}^{n_{SCA}} \Delta t_i = T_{SCA} = \frac{n_{SCA}}{f_{SCA}} \quad . \tag{2.8}$$

The Δt_b, the $\Delta t_{a,b}$ and the T_{SCA} are definitions which are mandatory for the reconstruction of the later introduced NEW-TCs.

In fig. 2.5 one can see that $n_{SCA} = 6$. With (2.8) one can calculate that T_{SCA} is 1.2 ns. Further, this SCA example consists of six Δt_b, from which two Δt_b are shown: $\Delta t_{5,6} \stackrel{!}{=} \Delta t_6 = 0.3\,\text{ns}$ and $\Delta t_{2,3} \stackrel{!}{=} \Delta t_3 = 0.1\,\text{ns}$. Additionally, one $\Delta t_{a,b}$ is illustrated: $\Delta t_{1,5}$ with a time difference of 0.9 ns between capacitor # 1 and capacitor # 5. $\Delta t_{1,5}$

[II] PSI uses a different nomenclature compared to (2.6). Their definition is $\Delta t_{b,b+1} \stackrel{PSI}{=} \Delta t_b$. The DRS4-manual does not provide this information. Only their provided C-code offers enlightenment.

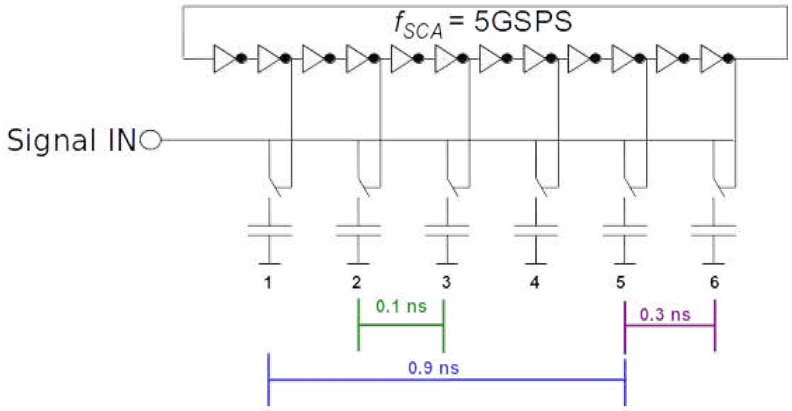


Figure 2.5: SCA consisting of 6 cells. Visible are also two local time differences ($\Delta t_6 = 0.3\,\text{ns}$ & $\Delta t_3 = 0.1\,\text{ns}$) and a global time difference ($\Delta t_{1,5}$ =0.9 ns).

can be calculated with (2.7) as $\Delta t_{1,5} = \Delta t_2 + \Delta t_3 + \Delta t_4 + \Delta t_5$ and is the sum of four Δt_b.

It should be noticed that an SCA is automatically calibrated in time if all Δt_b are known. This would result in the DRS4-case in a set of 1024 individual Δt_b. All NEW-TCs that are introduced in this work, are performed with a provided *Frequency which is used for the Time Calibration Signal* (f_{TC}). These periodic signals consist of rising and falling regions. Therefore a region dependent TC-method must be performed resulting in two sets of Δt_b. The *Final Set of* Δt_b ($end\Delta t_b$) can be calculated with the *Rising Edge Set of* Δt_b ($ris\Delta t_b$) and the *Falling Edge Set of* Δt_b ($fal\Delta t_b$) as

$$end\Delta t_b = (fal\Delta t_b + ris\Delta t_b) \cdot \frac{1}{2} \quad . \tag{2.9}$$

The resulting (2.9) cancels any residual voltage offsets and provides the final TC outcome (also called: TC table).

2.2.2 Frequencies Time Calibration (FTC)

Since the DRS4 was never calibrated correctly, all expectations of the chip behavior had to be questioned resulting in the *Frequencies Time Calibration* (FTC). As postulated the FTC solved all the DRS4-problems that originated from any previous TC-methods. However, the FTC is complicated and requires expensive equipment.

Superficially, the FTC consists of two parts. The first part provides multiple

$\Delta t_{a,b}$ by analyzing digitized oscillating signals. Afterwards, the second part utilizes all these measured $\Delta t_{a,b}$ and results in the calibration table[III].

The FTC requires multiple known f_{TC} and provides the opportunity to measure the true f_{SCA}. Thus, the expected f_{SCA} is not required to perform the FTC. The basic idea behind the FTC is that it works without any interpolation methods. For instance when digitizing a sine wave with a f_{TC} of $225.\overline{225}\,\mathrm{MHz}$, it is not very likely (but possible) that two far apart SPs digitize exactly the same voltage. In that case the time distance between the two SPs would be exactly a multiple of the period (one period = 4440 ps). In fig. 2.6 one can see such a case, where the global time difference between cell #25 and cell #94 is approximately $3 \times 4440\,\mathrm{ps} = 13.32\,\mathrm{ns}$. This is because the measured voltages of cell #25 (V_{25}) and cell #94 (V_{94}) are almost identical.

The *Tolerance Voltage for the FTC* (V_{FTC}) defines the allowed voltage difference between coincident SP-pairs. Thus, if a second measured voltage is inside the V_{FTC}, both SPs are considered to be a multiple of the period. For example a V_{FTC} of 4 mV fulfills the condition in fig. 2.6. One can see that the two SPs $V_{25} = -81\,\mathrm{mV}$ and $V_{94} = -81.9\,\mathrm{mV}$ result in $V_{FTC} > |V_{25} - V_{94}|$. Since a single f_{TC} only detects a small amount of matching $\Delta t_{a,b}$, the FTC utilizes multiple f_{TC}.

After the basic idea of the first part of the FTC is understood, the true $\Delta t_{a,b}$ can be calculated with the following: The FTC counts all $\Delta t_{a,b}$ of SP-pairs inside the V_{FTC} for all given periods (all f_{TC}). Afterwards, (2.10) utilizes all collected $\Delta t_{a,b}$ information as

$$\text{true } \Delta t_{a,b} = \frac{N_g \cdot \frac{m_g}{f_{TC_g}} + N_h \cdot \frac{m_h}{f_{TC_h}} + \cdots}{N_g + N_h + \cdots} \quad , \tag{2.10}$$

where N_g & N_h are the numbers of matching $\Delta t_{a,b}$ and $\frac{1}{f_{TC_h}}$ & $\frac{1}{f_{TC_g}}$ their corresponding periods. m_g and m_h are usually equal and stand for the multiples of the measured periods[IV].

Staying with the previous $225.\overline{225}\,\mathrm{MHz}$ example, a possible measurement for $\Delta t_{25,94}$, after analyzing all f_{TC} , could be the following: 90 times $3 \times 4440\,\mathrm{ps}$ and

[III] Nomenclatures like "calibration table" or "$\Delta t_{a,b}$" are explained in section, 2.2.1.

[IV] If more than two f_{TC} are detected for a single $\Delta t_{a,b}$, (2.10) has to be modified which is symbolized by the dots.

the neighboring f_{TC} detects 10 times 3×4450 ps between cell# 25 & cell# 94. By using (2.10), $\Delta t_{25,94}$ can be calculated as $\Delta t_{25,94} = \frac{90 \cdot 3 \cdot 4440\,\text{ps} + 10 \cdot 3 \cdot 4450\,\text{ps}}{100} = 13323\,\text{ps}$.

Further, the *Number of FTC frequencies* (n_{FTC}) together with the *Equidistant Period Difference* (t_{FTC}) define the *Maximum Calibration Range* (t_{max}). The t_{max} can be calculated as

$$t_{\text{max}} = (n_{\text{FTC}} - 1) \cdot t_{\text{FTC}} \ , \tag{2.11}$$

where n_{FTC} is the number of distinct f_{TC} that are used for the FTC and the t_{FTC} is the period time difference between two neighboring f_{TC}. Further, all digitized FTCs must follow the constrains in (2.26). An additional condition is that t_{max} must be greater than the longest Δt_b of a given f_{SCA}. Finally, the *Number of waveforms for one distinct TC frequency* (N_{wave}) must be identical for all applied FTC iterations (all f_{TC})! Detailed examples illustrating the t_{max} and the N_{wave} conditions are given in section 2.2.7.

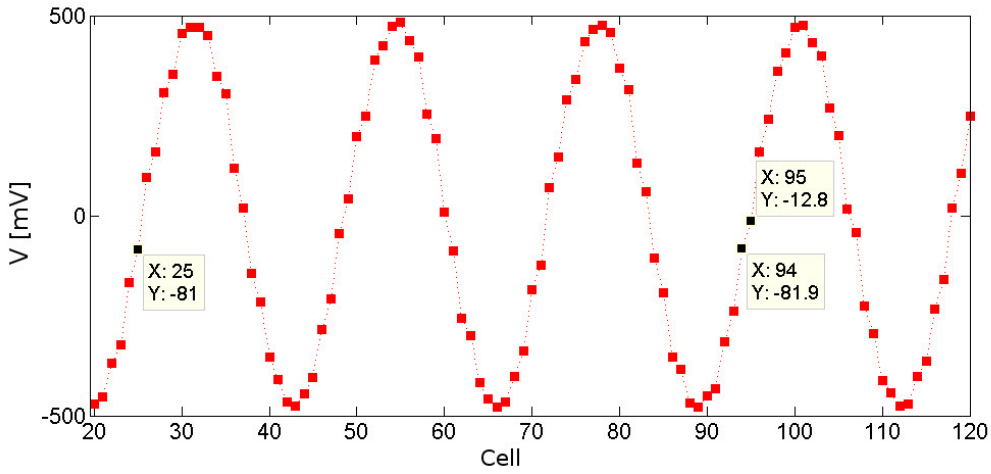


Figure 2.6: It shows the first 101 cells of the 1024 point-array of the DRS4. The chip is stopped at cell #20. Digitized are the sampling points of a sine wave with a FTC of $225.\overline{225}$ MHz. The DRS4 is running at an f_{SCA} of about 5 GSPS.

When analyzing the entire $n_{\text{FTC}} \times N_{\text{wave}}$ digitized waveforms with V_{FTC} and (2.10), one will compute a huge number (N) of distinct true $\Delta t_{a,b}$. The resulting set of equations consist of global time difference values (T_N) which are similar to the upper mentioned equation $\Delta t_{25,94} = 13323\,\text{ps}$. Further, the resulting set of equations in

(2.12) is the starting condition for the second part of the FTC.

$$\begin{aligned} \Delta t_{c,b} &= T_1 \\ \Delta t_{d,c} &= T_2 \\ &\vdots \\ \Delta t_{e,a} &= T_N \end{aligned} \tag{2.12}$$

The variables in (2.12) represent the cell#. In total there are as many variables as n_{SCA}. The variables a, b, c, d and e stand for values between 0 and 1023 in the DRS4 case. An alternative way of writing (2.12) using (2.7) is shown in (2.13), where all the neighboring time differences are summed up.

$$\begin{aligned} \Delta t_{c+1} + \Delta t_{c+2} + \cdots + \Delta t_{b-1} + \Delta t_b &= T_1 \\ \Delta t_{d+1} + \Delta t_{d+2} + \cdots + \Delta t_{c-1} + \Delta t_c &= T_2 \\ &\vdots \\ \Delta t_{e+1} + \Delta t_{e+2} + \cdots + \Delta t_{a-1} + \Delta t_a &= T_N \end{aligned} \tag{2.13}$$

For better understanding, the variables will be initialized with real numbers like that from a possible DRS4-FTC scenario: $a = 591$, $b = 91$, $c = 0$, $d = 940$ and $e = 478$.

$$\begin{aligned} \Delta t_{0,1} + \Delta t_{1,2} + \cdots + \Delta t_{89,90} + \Delta t_{90,91} &= 18.032\,\text{ns} \\ \Delta t_{940,941} + \Delta t_{941,942} + \cdots + \Delta t_{1022,1023} + \Delta t_{1023,0} &= 16.321\,\text{ns} \\ &\vdots \\ \Delta t_{478,479} + \Delta t_{479,480} + \cdots + \Delta t_{589,590} + \Delta t_{590,591} &= 22.187\,\text{ns} \end{aligned} \tag{2.14}$$

The before mentioned N is roughly predictable by the following formula

$$\frac{n_{SCA}^2 \cdot f_{TC_{slow}}}{f_{SCA}} < N < \frac{n_{SCA}^2 \cdot f_{TC_{fast}}}{f_{SCA}}, \tag{2.15}$$

where $f_{TC_{slow}}$ is the slowest and $f_{TC_{fast}}$ is the fastest of the n_{FTC} frequencies. For example a DRS4 running at $f_{SCA} = 5\,\mathrm{GSPS}$ and $f_{TC_{fast}} = 250\,\mathrm{MHz}$ a system of approximately 50,000 equations would be expected for each edge region. Thus, after solving two systems of linear equations one will result in $ris\Delta t_b$ and $fal\Delta t_b$ for a given f_{SCA}. Afterwards, the final TC outcome can be calculated by (2.9).

By solving this system of linear equations, the second part of the FTC is completed. By combining both parts the first successful approach with regards to calibrating the DRS4-chip was established. Although it is a tedious task to write the C-code which analytically solves this system of linear equations, it will not be expanded in the following lines. However, the solution can be extracted from the C-code of this work. Alternate options utilizing a numerical approach are also possible and explained in section 2.2.4. These possibilities are also easier to implement and require less resources with respect to memory usage and computation time.

The FTC will theoretically work for any SCA running at any f_{SCA}. However, the FTC is expensive and challenging to implement. Therefore, another TC-technique is favored that uses less FTC frequencies and ideally avoids the need of solving a system of linear equations. This goal has also been accomplished in this work and the theory will be explained in more detail in the following two sub-sections.

2.2.3 Local Time Calibration (LTC)

The *Local Time Calibration* (LTC) was developed independently by the author as an alternative TC-method for SCA-chips. At least two publications[74, 96] have already introduced the basic idea, but with different realizations.

Originally, the LTC was developed as a standalone solution to replace the previous introduced FTC from section 2.2.2 . Finally, it became the first part of a two-part FTC-replacement. The LTC also requires less additional hardware compared to the FTC and is relatively easy to implement. If necessary the LTC can be utilized as standalone-algorithm, but the TC outcome is insufficient if the algorithm is not applied correctly. Additionally, if the true f_{SCA} of the SCA is not known, the LTC will result in a systematic time error. Both mentioned mistakes are reproduced in this work and can be found in fig. 3.26(a & b).

The LTC focuses on the identification of the $end\Delta t_b$ as it is defined in section 2.2.1. In particular the LTC-approach considers a Δt_b to be equivalent to its corresponding ΔV_b when applying a linear increasing or decreasing signal. The only requirement is that the applied signal has a relatively constant slope. One could think of a sawtooth shape signal for example as shown in fig. 2.7. Consequently, the

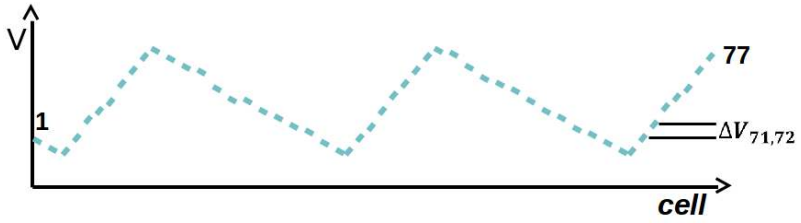


Figure 2.7: It shows an SCA with 77 cells. One can see that the SPs are not equidistant. Since the sawtooth signal has a linear behavior $\Delta V_{71,72}$ has to be equivalent to $\Delta t_{71,72}$.

sum of all ΔV_b is equivalent to the sum of all Δt_b. The intercept theorem results in (2.16) and is illustrated in fig. 2.8.

$$\frac{\Delta t_i}{\Delta V_i} = \frac{\sum \Delta t_i}{\sum \Delta V_i} \tag{2.16}$$

$\sum \Delta t_i$ can be calculated with the f_{SCA} and the total number of sampling cells (n_{SCA}) as:

$$\sum_{i=1}^{n_{SCA}} \Delta t_i = \frac{n_{SCA}}{f_{SCA}}. \tag{2.17}$$

The combination of (2.16) and (2.17) provides the solutions for the LTC as

$$\Delta t_i = \frac{\Delta V_i \cdot n_{SCA}}{\sum \Delta V_i \cdot f_{SCA}}. \tag{2.18}$$

If only the LTC is used as a standalone method, (2.18) has to be applied n_{SCA} times for each edge, individually ($fal\Delta t_b$ and $ris\Delta t_b$). Thus, for the DRS4 case, one would calculate all 1024 Δt_b twice. Afterwards, the correct local time differences can be calculated by making use of (2.9).

The exact f_{SCA} is normally not required because it will be determined with the second part of the FTC-replacement which is described in section 2.2.4. Since the LTC does not have to be perfectly correct one can simply use the rising and falling

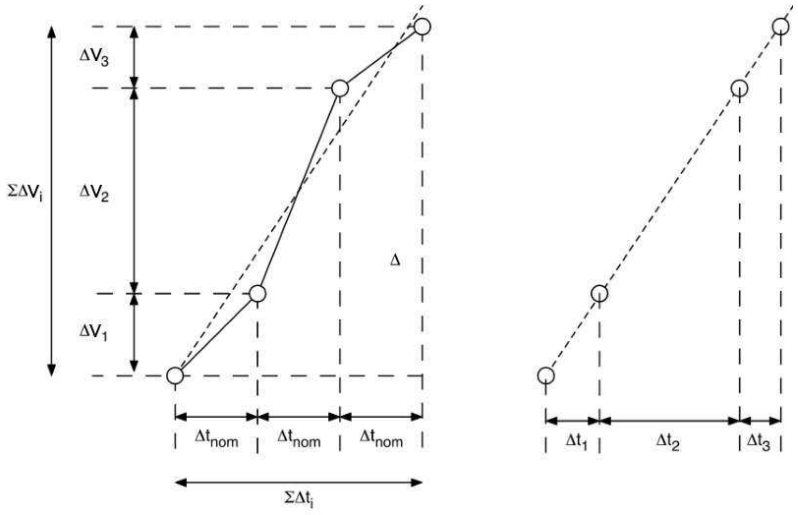


Figure 2.8: Correlation between ΔV_i and Δt_i illustrated on a sampled rising edge with equidistant (a) and true sampling intervals (b). Figure taken from [31].

edges of a sine wave like the one in fig. 2.6. The δ_{lin} which appears because of this not-optimal sine wave signal is simulated and can be found in fig. 2.11. The results are discussed in section 4.3.

2.2.4 Global Time Calibration (GTC)

The *Global Time Calibration* (GTC) was implemented because the LTC from the previous section 2.2.3 provides correct results only to a certain extent. More details are discussed in section 4.3.

Further, the GTC is an improved version of the already introduced FTC (see section 2.2.2). Instead of applying multiple frequencies it functions with a single periodic signal. The LTC combined with the GTC is the perfect FTC-replacement, because both can utilize the same f_{TC}. The f_{TC} restrictions are available from (2.26).

Like the FTC, the GTC consists of two parts. Its first part provides the same output as the first part of the FTC. From here on starts the second part. Thus, either the second part from the FTC can be utilized or other solutions can be taken into consideration which will be introduced later.

The LTC output ($end\Delta t_b$) is needed to deliver an *Initial Set of* Δt_b ($ini\Delta t_b$). One can also utilize the GTC as standalone version when utilizing (2.27). The first part

of the GTC can be utilized with one of these two initial conditions.

The first part of the GTC distinguishes between two similar methods. One method is called the single-sided correction and the formula can be found in (2.19).

$$\frac{m}{f_{TC}} \stackrel{!}{=} \Delta t_{x,y} - t_{cor} \quad \text{with} \quad t_{cor} = \frac{V_y - V_x}{\Delta V_y} \cdot \Delta t_y. \tag{2.19}$$

V_x & V_y are the voltages measured in cell $\#x$ & cell $\#y$ with $V_x < V_y$. m stands for the multiple of the measured period. When applying (2.16), ΔV_y is $(V_y - V_{y-1})$. Thus (2.19) provides the correction in time (t_{cor}) between the expected period time ($\frac{m}{f_{TC}}$) and the measured time ($\Delta t_{x,y}$).

For better understanding of the single-sided correction the previously shown example in fig. 2.6 is used. One can see that $\Delta t_{25,95}$ must be greater than 13.32 ns, because $V_{25} = -81$ mV lies in between V_{94} & V_{95}. Thus, (2.19) will provide the t_{cor} by making a linear interpolation between cell# 94 and cell# 95 with Δt_{95}. Δt_{95} can be estimated with (2.27). When using $x = 25$, $y = 95$ and Δt_{95} ≈200 ps, one can calculate t_{cor} with (2.19). Thus, $t_{cor} = \frac{-12.8+81}{-12.8+81.9} \cdot 200\,\text{ps} \approx 197\,\text{ps}$. Finally, (2.19) results in $\Delta t_{25,95} = 3 \cdot 4440\,\text{ps} + 197\,\text{ps} = 13.517\,\text{ns}$ with f_{TC} $225.\overline{225}$ MHz.

An alternative to the single-sided correction in (2.19) is the double-sided correction in (2.20), which calculates the period of a chosen reference voltage (V_{ref}). The double-sided correction uses two linear interpolations as

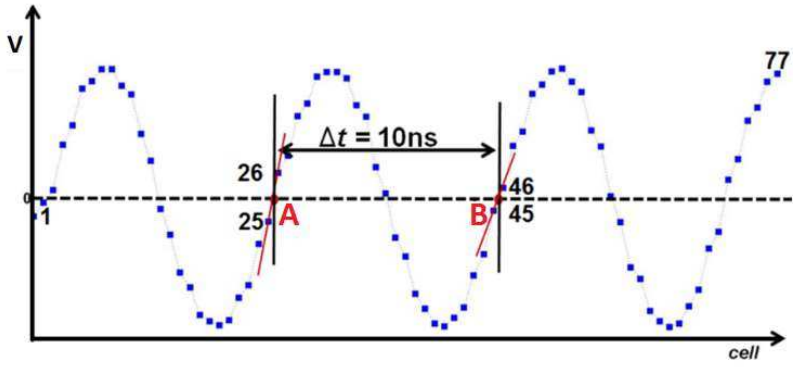


Figure 2.9: Digitized are the SPs of a 100 MHz sine wave. Shown are the first 77 SPs of 1024 SPs. The DRS4 is running at an f_{SCA} of 2.5 GSPS. One can see that the $\Delta t_{A,B}$ must be 10 ns.

$$\frac{m}{f_{TC}} \stackrel{!}{=} \Delta t_{x,y} - t_{cor} \quad \text{with} \quad t_{cor} = \frac{V_y - V_{ref}}{\Delta V_y} \cdot \Delta t_y - \frac{V_x - V_{ref}}{\Delta V_x} \cdot \Delta t_x. \tag{2.20}$$

V_x and V_y are defined to be the greater than V_{ref}. A V_{ref} of 0 V with a defined period of 10 ns is illustrated in fig. 2.9. Thus, for the given example in fig. 2.9 the variables $x = 26$ and $y = 46$ would be used in (2.20).

When analyzing all combinations of $\Delta t_{a,b}$ which originate from the digitized waveforms either by applying (2.19) or by utilizing (2.20) one will result in multiple t_{cor}. The total amount t_{cor} is equal to the *Number of all expected* $\Delta t_{a,b}$ (n_{all}) and can be computed as

$$n_{\text{all}} = T_{SCA} \cdot f_{TC} \, (T_{SCA} \cdot f_{TC} - 1) \cdot \frac{N_{\text{wave}}}{2} \qquad \text{with} \qquad T_{SCA} \cdot f_{TC} \in \mathbb{Z}^+ \tag{2.21}$$

All t_{cor} can be iteratively applied to the $ini\Delta t_b$ which forms the second part of the GTC. There are two possibilities to utilize the t_{cor} information. Either by multiplying the $ini\Delta t_b$ with a *Correction Unit* (u_{cor}) as

$$\begin{aligned}
res\Delta t_{x+1} &= ini\Delta t_{x+1} \cdot u_{cor} (\star\star) \\
res\Delta t_{x+2} &= ini\Delta t_{x+2} \cdot u_{cor} \\
&\vdots \qquad\qquad \text{with} \quad u_{cor} = \frac{m}{f_{TC} \cdot (\Delta t_{x,y} - t_{cor})} \\
res\Delta t_{y-1} &= ini\Delta t_{y-1} \cdot u_{cor} \\
res\Delta t_{y} \quad &= ini\Delta t_{y} \quad \cdot u_{cor} (\star)
\end{aligned} \tag{2.22}$$

or adding a *Correction Value* (v_{cor}) to the $ini\Delta t_b$ as

$$\begin{aligned}
res\Delta t_{x+1} &= ini\Delta t_{x+1} + v_{cor} (\star\star) \\
res\Delta t_{x+2} &= ini\Delta t_{x+2} + v_{cor} \\
&\vdots \qquad\qquad \text{with} \quad v_{cor} = \frac{\frac{m}{f_{TC}} - (\Delta t_{x,y} - t_{cor})}{y - x} \\
res\Delta t_{y-1} &= ini\Delta t_{y-1} + v_{cor} \\
res\Delta t_{y} \quad &= ini\Delta t_{y} \quad + v_{cor} (\star)
\end{aligned} \tag{2.23}$$

where $ini\Delta t_{x+1} \cdots ini\Delta t_y$ stand for the initial dataset of local time differences that are going to be corrected and consequently $res\Delta t_{x+1} \cdots res\Delta t_y$ stand for the resulting local time differences. The usage of the last equation labeled with a star ($\star$) is optional for (2.20) and (2.19). It basically defines if the last Δt_b of a measured $\Delta t_{a,b}$ will be changed, too. The usage of the first equation labeled with two stars ($\star\,\star$) is only optional for (2.20). That means, ($\star\,\star$) is mandatory when using (2.19). If the equations labeled with ($\star$) or ($\star\,\star$) are chosen not to be used, $\Delta t_{x,y}$ has to be modified in (2.22) and (2.23). Additionally, $y - x$ has to be decreased in (2.23). This is because the investigated $\Delta t_{a,b}$ will decrease automatically for every missing equation [V].

Summarized, the second part of the GTC always starts with $ini\Delta t_b$ (e.g. provided by LTC). In the following iterations the *Resulting Set of* Δt_b ($res\Delta t_b$) provided by (2.22) or (2.23) will be reused as $ini\Delta t_b$ in order to repeat the procedure until the GTC outcome is sufficient.

Obviously there are a lot of combinations possible when utilizing the GTC. All have their advantages and disadvantages and have been analyzed in this work. In section 4.3 one will find a discussion concerning the evaluated GTC-combinations.

The most promising GTC-combination utilizes an optimization of (2.19) and is used for all applied GTCs in this thesis. Instead of using $\Delta t_{x,y}$ in (2.19), calculated are its mean values $\Delta\bar{t}_{x,y}$ while keeping $\Delta\bar{t}_y$ as an unknown fraction and applying them afterwards to (2.23) without the equation labeled with ($\star$). Two advantages result from using $\Delta\bar{t}_{x,y}$. First, $\Delta\bar{t}_{x,y}$ offers the possibility of rejecting so-called outliers (wrong $\Delta t_{x,y}$ that do not fit in the distribution of $\Delta\bar{t}_{x,y}$). The other advantage is that the array of $\Delta\bar{t}_{x,y}$ can be applied as often as required until a satisfying result is achieved. Independent of the N_{wave}, f_{SCA} and f_{TC} one can predict the allocated memory (mem) as

$$mem = n_{SCA} \times n_{SCA} \times mem_{unit}, \tag{2.24}$$

where mem_{unit} is the required memory in bits for a single storage cell. With (2.15) and f_{TC}, one can calculate the expected amount of storage cells where mea-

[V] Note: Also the second part of the FTC can be replaced by (2.22) or (2.23). In this case, no star-equation can be left out.

sured $\Delta\bar{t}_{x,y}$ are expected. With an f_{TC} of 100 MHz and running the DRS4-chip at f_{SCA}=5 GSPS, one can expect 20,000 measured $\Delta\bar{t}_{x,y}$ inside the internal memory for each of the two edge regions. A possible way to allocate this high amount of memory for the storage cells is to restrict the discrete measurements (e.g. 1000). With this approach one would waste measurements and therefore a better method is developed in this thesis to collect endless measurements. The method maintains the possibility of rejecting outliers and allocates a minimum amount of memory for a single storage cell. More details about this method are given in section 2.1.5.

2.2.5 Signal Requirements to Perform the NEW-TCs

The three NEW-TCs that are described in the previous three sub-sections require analog input signals. These signals have to be digitized by the channel of the SCA that will be calibrated. Care has to be taken that the *Stop Cell of the SCA* (c_{stop}) information[VI] is saved with every TC-measurement. Thus, when calibrating one channel of the DRS4-chip, 1024 SPs and a dedicated c_{stop} would be saved for one waveform. All 9 channels of the DRS4 have the same c_{stop}. Therefore, all channels can be calibrated at once. However, for ideal TC-results, where every picosecond counts, it is recommended to calibrate an SCA channel-by-channel to avoid cross-talk between the channels. The function generators, which are used to produce TC-signals in this work are the *Tabor Waveform Generator Model WW2571A* (W2571) and the *Tektronix Arbitrary/Function Generator AFG3251* (W3251).

For the LTC, a linearly behaving signal, e.g. a sawtooth signal, is best. If the BW is considered identical for all SPs, the frequency is irrelevant in this case. Still, a faster f_{TC} has advantages. The TC-duration will decrease as a result, because more usable SPs are available from a single waveform and additionally a better SNR is expected. If the LTC is used in combination with the GTC, a sine wave is recommended as input signal. The shape of a sine wave around the zero crossings is almost linearly behaving as required for the LTC. Nevertheless it will result in a δ_{lin} which is dependent on the f_{TC}. The δ_{lin} also depends on the Δt_b and can be predicted as a time walk between the fastest zero crossing and the slowest zero

[VI] An example of two individual c_{stop} scenarios is provided in section 2.3.8.

crossing as

$$\delta_{lin} = \Delta t_b \cdot \left(1 - \frac{\sin(2\pi \cdot f_{TC} \cdot \Delta t_b)}{2 \cdot \sin(2\pi \cdot f_{TC} \cdot \Delta t_b/2)}\right). \tag{2.25}$$

A simulation of the sine wave error is shown in fig. 2.11(e & f) utilizing (2.25) for three f_{TC}. Alternatives to signal generators are pocket pulsers, like the *Phillips NIM Pocket Pulser model 417* (P417). Although this solution is very cheap, it would result in a time-consuming LTC, since only one edge with a few SPs would be usable from each waveform.

The two other methods, FTC and GTC, require periodic signals where the exact f_{TC} must be available with a low time jitter. When digitizing the periodic signal the resulting waveform provides multiple $\Delta t_{a,b}$. Considered should only be a $\Delta t_{a,b}$ measured between linearly behaving oscillating regions like the rising edges which are shown in fig. 2.6. The time between two neighboring edges, e.g. falling edge and rising edge, is not necessarily half the period! This was reproduced by measurements of all function generators in house. Also measured was that the oscillating signals with the lowest time jitter are sine waves. Therefore, only sine waves of f_{TC} in the MHz-regions are generated and digitized for all NEW-TCs of this work. An SCA with a given n_{SCA} running at f_{SCA} has the following f_{TC}-options:

$$f_{TC} \in \left[\frac{2}{n_{SCA}} f_{SCA}, \frac{1}{10} f_{SCA}\right] \tag{2.26}$$

Based on the results of this work, the f_{TC}-options in (2.26) have been slightly increased compared to the formula in Stricker-Shaver et al[31]. (2.26) provides the f_{TC} according to the sampling speed range of the SCA. For example a DRS4 range from 0.7 GSPS to 5 GSPS results in an f_{TC} of 70 MHz. 70 MHz is the highest possible frequency due to (2.26) for the critical 0.7 GSPS case. If the frequency is higher, the linear interpolation in the LTC algorithm would break down for the 0.7 GSPS case. If the frequency is lower, the duration of the TC would needlessly increase.

2.2.6 Alternative Time Calibrations

All SCAs consist of different sets of Δt_b which have to be calibrated, e.g. with the NEW-TC. The *Assumption of Equidistant Sampling Points* (NO-TC) assumes

equidistant sampling intervals as coming from a real ADC. In this case the $end\Delta t_b$ can be predicted as

$$end\Delta t_b = \left[\frac{1}{f_{SCA}}, \frac{1}{f_{SCA}}, \cdots, \frac{1}{f_{SCA}}\right]. \tag{2.27}$$

Thus, for the DRS4 case all 1024 Δt_b correspond to 200±0 ps when sampling at an f_{SCA} of 5 GSPS.

The *DRS4 Evaluation Board version 3* (V3) utilizes the *TC-method provided by the V3* (V3-TC). It uses an 240 MHz clock which is produced internally in the V3. It also measures the periods similar to the GTC. First a simplified version of (2.20) with V_{ref} equal to 0 V is applied. Afterwards the V3-TC corrects all 1024 Δt_b. This procedure is repeated each time a period is measured. The correction procedure continues until the set of Δt_b fulfills the calibration condition. It is fulfilled when measured periods are within a given error value. The algorithm can be found in the provided C-code from PSI.

Starting with the *DRS4 Evaluation Board version 5* (V5), the *TC-method provided by the V5* (V5-TC) was established. The V5-TC utilizes 1000 digitized sine waves coming from an additionally placed low-jitter 100 MHz clock. The 100 MHz clock is the main hardware change compared to the previous version of the DRS4 Evaluation Board series. The updated hardware and improved calibration software, the V5-TC, is exclusively influenced by this thesis. The V5-TC consists of an combination of the LTC and the GTC. Stefan Ritt from PSI triggered the work on the GTC and afterwards adopted one combination of the NEW-TCs, the here-called V5-TC. First the LTC is applied together with the mentioned 1000 digitized sine waves resulting in $end\Delta t_b$. Afterwards, when applying the GTC together with another 1000 collected sine waves the LTC-result successively improves. His chosen GTC settings use the (2.20) in combination with (2.22). Further, the V_{ref} is set to 0 V and thus only zero-crossings are utilized. The V5-TC is applied to every channel of the V5. More information about the V5-TC can be found in the provided C-code from PSI.

The default settings for the *742-Series Board Based on DRS4-chip from CAEN*

(X742) utilize the CAEN calibrations directly, while the signals are digitized. Afterwards, the SPs become equidistant through linear interpolation of the digitized SPs. For this interpolation the time table computed by the *TC-method provided by CAEN* (CAEN-TC) is required. The CAEN-TC table is permanently stored in the flash memory. The same time table is applied to all channels of an individual DRS4-chip. Thus, the V1742 has 12 stored time tables (4 DRS4-chips × 3 f_{SCA}). The user manual from CAEN provides no information how the CAEN-TC is performed in the CAEN facility.

2.2.7 Comparison of the Most Relevant TCs and NEW-TCs

The most relevant NEW-TCs for SCAs are utilized exclusively with the DRS4-chip which is an SCA representative. As illustrated in the previous four sub-sections a variety of possible TC-method combinations can be tested. All combinations that are left out, showed worse or equal performance compared to the following that were chosen. All results comparing the most relevant NEW-TCs can be found in section 3.3.1. Compared are dedicated settings for LTCs, GTCs, a combination of both and FTCs. Additionally, the NEW-TC is compared repeatedly to the V3-TC, the V5-TC, the CAEN-TC and the NO-TC in chapter 3.

All utilized signals for the NEW-TCs are sine waves ranging from 30 MHz to 239 MHz with a 1 V peak-to-peak value. For comparison reasons, the condition N_{wave}=1000 is fulfilled for all NEW-TCs. This sums up to around 1 million available SPs to perform a TC-method (1024 SPs ×1000 waveforms).

One possible abbreviation that describes a NEW-TC setting would be "100 MHz LTC". It means that a sine wave with an f_{TC}= 100 MHz is digitized 1000 times to perform the LTC. Since all NEW-TCs utilize multiple SPs along the edge of the zero crossing, one has to regulate the SPs by their quality. This is done by defining a *Symmetric Voltage limit for the TC signal* (V_{max}). Thus, if $|V_{SP}| > V_{max}$, the SP will be ignored for the TC-method. Except for the FTC, linear interpolations are performed for the NEW-TCs. The ideal V_{max} is 100 mV for a linearly interpolated f_{TC} of 100 MHz. This is simulated for the DRS4 with f_{SCA}=5.12 GSPS. The simulation results are illustrated in fig. 2.10. Only for the (100 MHz @ 5.12 GSPS)-case

is the ideal V_{max} simulated. For other f_{SCA} and f_{TC} combinations, the ideal V_{max} changes, and is calculated with (2.28) in this work. (2.28) does not provide the optimal value like that from a simulation. However, it is a good starting point and calculates the minimum value of V_{max} as

$$V_{max} > \frac{V_{PtP}}{4} \cdot \sin(2\pi \cdot f_{TC} \cdot \max\Delta t_b), \tag{2.28}$$

with V_{PtP} being the peak-to-peak voltage of the sine wave and $\max\Delta t_b$ standing for the maximum Δt_b of a given f_{SCA}. Further, the $\max\Delta t_b$ of the DRS4 can be predicted as

$$\max\Delta t_b \approx \frac{2}{f_{SCA}}. \tag{2.29}$$

The first validation of (2.29) was performed in combination with the FTC and a sophisticated function generator. In particular, the W3251[97] was used to generate frequencies around 200 MHz. Further, starting with the fastest f_{TC} that was used for the FTC, each additional and slower f_{TC} was precisely 10 ps longer than the one before. In other words, the t_{FTC} was 10 ps for this scenario. The DRS4-chip was sampling with around 5 GSPS, when the first successful FTC was performed. Thus, a Δt_b of around 200 ps was expected. Nevertheless, a $t_{\max}$ of 290 ps failed and caused the C-code of the FTC to crash. The C-code crashes if a Δt_b cannot be calculated with the FTC-algorithm. This means that an initial $t_{\max}$ of 290 ps was too low. Therefore, n_{FTC} was increased until the C-code stopped crashing. After randomly increasing to 43 distinct frequencies with a t_{FTC} of 10 ps, the first FTC was functioning. Summarized, a $t_{\max}$=420 ps and a $\max\Delta t_b$=378 ps was measured which confirms the formula in (2.29). This first validation of (2.29) was time-consuming because the maximum Δt_b when sampling at 5 GSPS was not around 210 ps as expected but around 400 ps.

One of the most relevant NEW-TCs is exactly this mentioned FTC with the 43 distinct frequencies. The tested FTCs are labeled with the n_{FTC} including the voltage level information. The just mentioned FTC is therefore labeled as “43 frequencies FTC with 1 level”. Also tested in this work is an 11 and a 4 frequencies FTC. The 11 frequencies FTC utilizes a $t_{\max}$=400 ps and a t_{FTC}=40 ps. The 4

frequencies FTC utilizes a $t_{\max}$=420 ps and a t_{FTC}=140 ps. All FTCs use the same pool of multiple digitized f_{TC} which starts with the slowest f_{TC} of around 217 MHz and decreases in 10 ps-steps to the fastest $f_{TC}\approx$239 MHz. Thus, the 43 distinct frequencies are digitized with a random trigger. Each frequency fulfills the condition N_{wave}=1000. The FTC needs at least two FTC frequencies. In practice for this available pool of 43 frequencies the minimum amount is 4 frequencies. To utilize the FTC with only 2 frequencies, the noise of the FTC frequencies must be increased to create overlapping period regions.

The reason that the first FTC (43 frequencies FTC with 1 level) started with only one voltage level is that everything about the DRS4-chip was questioned. Only the fluctuation around the baseline level was trusted because it always resulted in the same outcome. Thus, the mentioned single voltage level lies at 0 mV with $V_{FTC} = \pm 3$ mV. V_{FTC} depends on the noise of the digitized signal and the t_{FTC}. Therefore, it is recommended to adjust V_{FTC} to get optimal results. Additionally, the voltage levels are always located symmetrically around the baseline level.

However, a 43 frequencies FTC with 101 voltage levels distributed equidistantly from -55 mV to 55 mV is also analyzed. The same settings with 101 levels (-55 mV to 55 mV) and additional 250 levels ranging from -260 mV to 260 mV were tested for the 11 frequencies FTC. 100 levels ranging from -150 mV to 150 mV were preset for the 4 frequencies FTC. When utilizing more than 1 level for the FTC algorithm, one should limit the SPs to the linearly behaving regions. For example an f_{TC} of 240 MHz where the peak-to-peak frequency deviation is 1000 mV, the maximal voltage levels of $\pm$150 mV ($\delta_{lin}\approx$ 2 ps) are recommended. The maximal voltage levels can be calculated with (2.25). Finally, for all FTCs in this thesis the analytical path is utilized [VII].

All tested GTCs use the same settings regardless of being utilized as a standalone version or in combination with the LTC. The GTC is only used in combination with $\Delta\bar{t}_{x,y}$ as it is explained at the end of section 2.2.4. This restricts the first part of the GTC to the single-sided GTC described by (2.19). Further, all considered $\Delta t_{a,b}$ are

[VII] Note: All TC-methods that provide in the first part a set of $\Delta t_{a,b}$, like FTC, (2.19) or (2.20) can in a second part utilize either the analytical solution, (2.22) or (2.23).

Table 2.1: Illustrated are the investigated TC-methods utilized with the DRS4-chip for three f_{SCA}-cases (≈1 GSPS, ≈2 GSPS and ≈5 GSPS).

row	TC-method	≈1 GHz	≈2 GHz	≈5 GHz	source
1	NO-TC	X	X	X	fig. 3.2
2	V3-TC	X	X	X	fig. 3.3
3	V5-TC	-	-	X	section 3.5.1
4	CAEN-TC	X	X	X	fig. 3.20
5	100MHz (3 to 10000) GTC	-	-	X	fig. 3.25(a-b)
6	30-217MHz LTC	-	-	X	fig. 3.26(a-b)
7	4 to 43 frequencies FTC	-	-	X	fig. 3.26(c-f)
8	30-217MHz LTC+3GTC	X	X	X	mostly

less than $\frac{3}{4}$ of the T_{SCA}. Thus, for an f_{TC}= 100 MHz and f_{SCA}= 5 GSPS, the 1st period to the 15th period are accepted. For the second part of the FTC an unlimited number of corrections is theoretically available. For simplicity 10,000 corrections are considered as a single GTC iteration. One correction is a random picked $\Delta\bar{t}_{x,y}$ out of all available $\Delta\bar{t}_{x,y}$. Every randomly picked new $\Delta\bar{t}_{x,y}$ must be calculated first before the correction is applied. The corrections are applied according to (2.23) without the equation labeled with a star ($\star$). It should also be noticed that all multiples of periods (e.g. 100 MHz) that fluctuate between two possibilities get either rejected or corrected by a dedicated algorithm. This is particularly the case for noisy cells or for cells with short Δt_b. Most GTC iterations are repeated 3 times (3 iterations = 3 × 10000 GTC corrections) which is symbolized by " 3GTC".

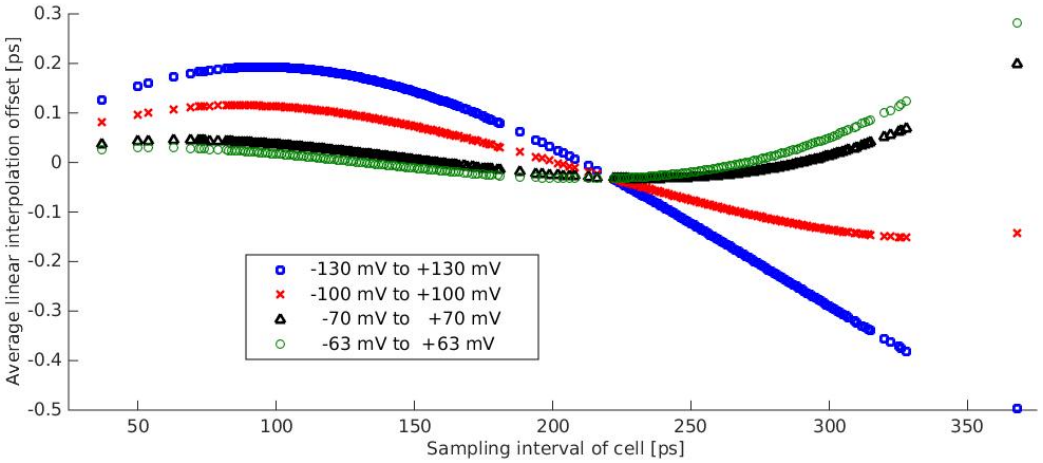
The *Reference method for NEW-TCs consisting of a LTC + 3GTCs* (LTC+3GTC) is chosen to be the reference method for the NEW-TCs. Thus, if not specifically mentioned the terminology " NEW-TC" refers to " f_{TC} LTC+3GTC" with a typical f_{TC} of 100 MHz. To be accurate the abbreviation LTC+3GTC consists of a combination of the LTC and the 3GTC utilizing the same f_{TC}. Table 2.1 provides a summary of all tested TC-methods. One can see in row #8 that the LTC+3GTC is utilized in most cases and for all f_{SCA}.

2.2.8 Simulated NEW-TC Errors and Settings

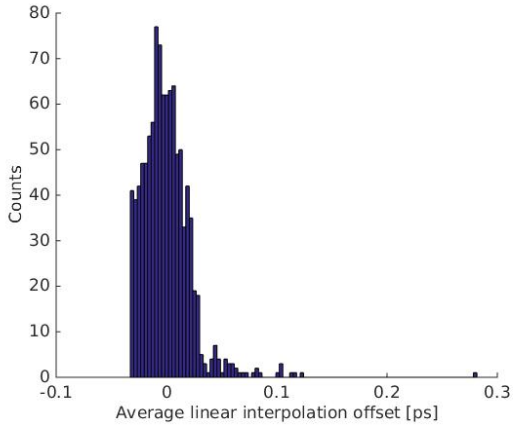
In fig. 2.10 one can see the simulated systematical error of δ_{lin}. This error symbolizes the average offset from the true Δt_b when applying a 2-points interpolation which in turn is permanently used for the GTC. For the simulation the DRS4 is running at a sampling speed of 5.12 GSPS in combination with a 100 MHz sine wave. Each computed error is the average error resulting from an individual Δt_b for a given V_{max}. The meaning of V_{max} is explained in section 2.2.7. The set of 1024 Δt_b is taken from a calibrated DRS4. One can see in fig. 2.10(a) that different Δt_b result in different average errors. The average errors are the systematic offsets from the true time that is calculated with the linear interpolation. The greatest interpolation error is 0.5 ps for a Δt_b around 380 ps and a given V_{max}=130 mV. In fig. 2.10(b - e) one will find the occurrence of each Δt_b error.

Illustrated in fig. 2.10(d) is the most symmetric error distribution with a V_{max} of 100 mV. The other shown simulation examples (b, c & e) result in a worse balanced error compared to (d). Caused by this simulation result, a V_{max}=100 mV is used for the NEW-TC when utilizing a f_{TC} of 100 MHz at 5.12 GSPS. The second best simulation result is (b) with V_{max}=63 mV. It also symbolizes the smallest possible V_{max} and can be calculated with (2.28).

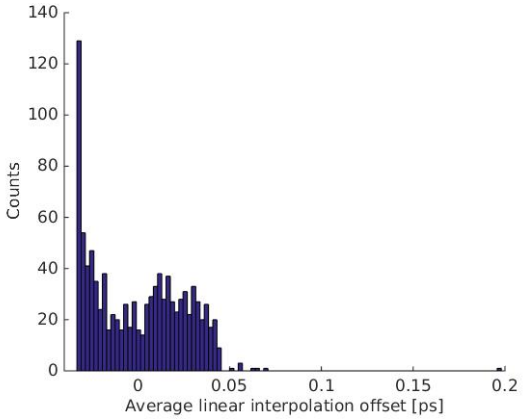
In fig. 2.11(a) n_{all} versus the TC frequency is plotted for N_{wave}= 1 utilizing (2.21). For other N_{wave}, n_{all} is plotted for three sine waves frequencies (30 MHz, 100 MHz and 240 MHz) in fig. 2.11(b). In both cases the DRS4 is running at 5.12 GSPS. Fig. 2.11(c & d) shows the waveforms of three f_{TC} that have been utilized for the NEW-TC in this work. Available is the time from 0 ps to 1600 ps (c) and a zoom in from 0 ps to 400 ps (d). Additionally provided in fig. 2.11(e & f) is a simulation utilizing (2.25). It shows the δ_{lin} for the three mentioned f_{TC} versus the Δt_b.



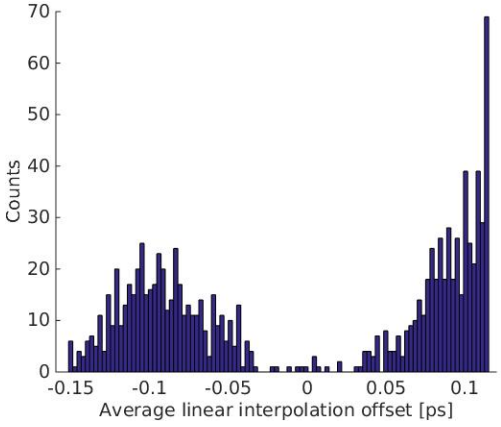
(a) 100 MHz error for 4 cases



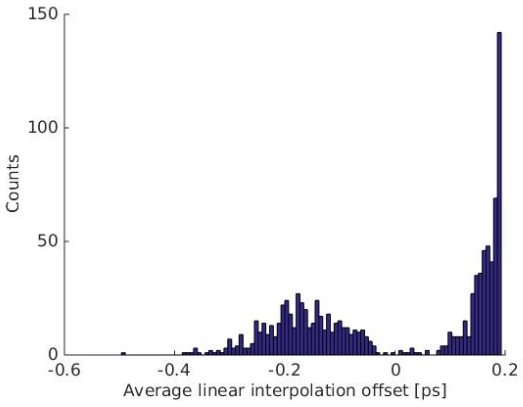
(b) +63 mV to -63 mV range



(c) +70 mV to -70 mV range

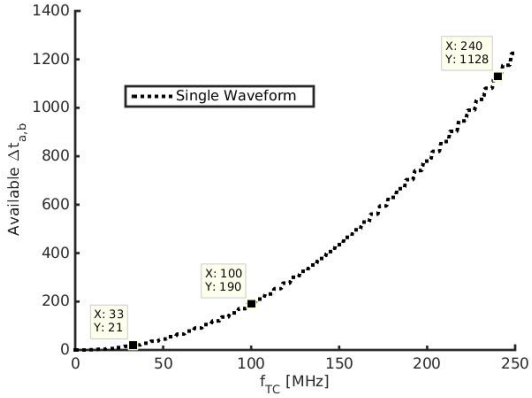


(d) +100 mV to -100 mV range

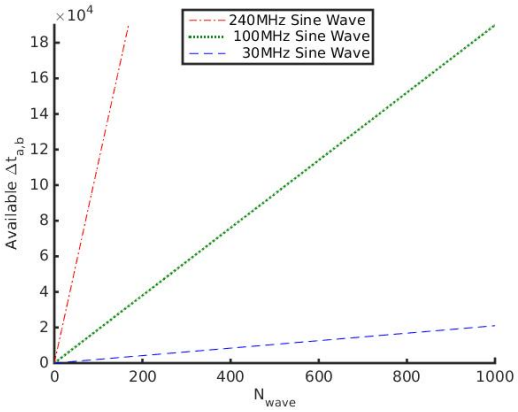


(e) +130 mV to -130 mV range

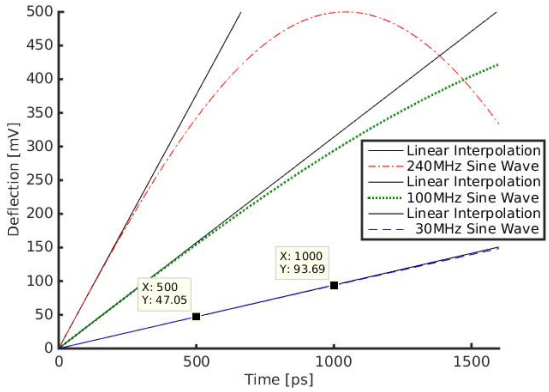
Figure 2.10: Simulated interpolation error for NEW-TC of DRS4 for 5.12 GSPS. (a) illustrates four V_{max} scenarios and (b-e) provide more details of the individual scenarios.



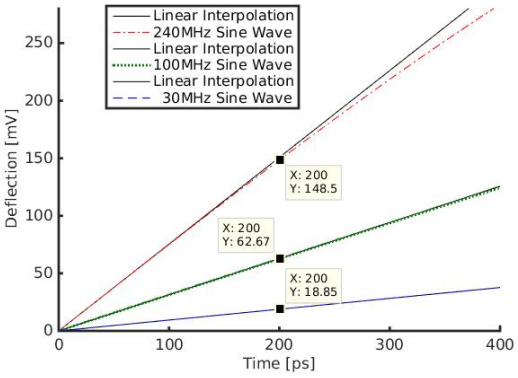
(a) Available $\Delta t_{a,b}$ for a single waveform



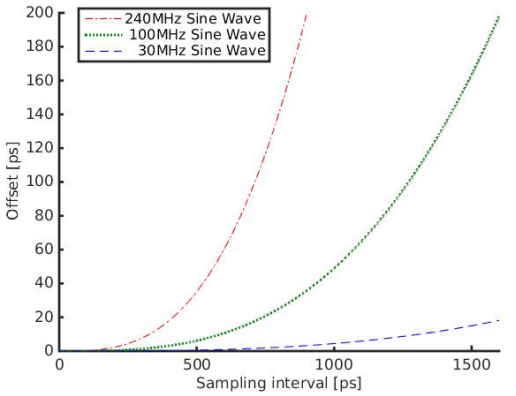
(b) Available $\Delta t_{a,b}$ up to 1000 waveforms



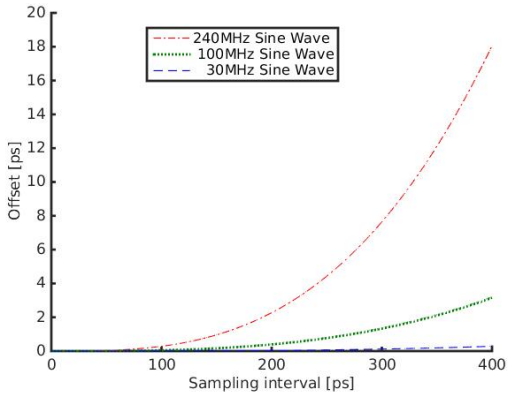
(c) Sine wave deflections up to 1.6 ns



(d) Sine wave deflections up to 0.4 ns



(e) Linear interpolation error up to 1.6 ns



(f) Linear interpolation error up to 0.4 ns

Figure 2.11: Shown in (a & b) are simulations of available $\Delta t_{a,b}$ for the DRS4 (5.12 GSPS). Additionally, one will the find a cutout of three sine wave curves (c & d) and their corresponding linear interpolation errors (e & f).

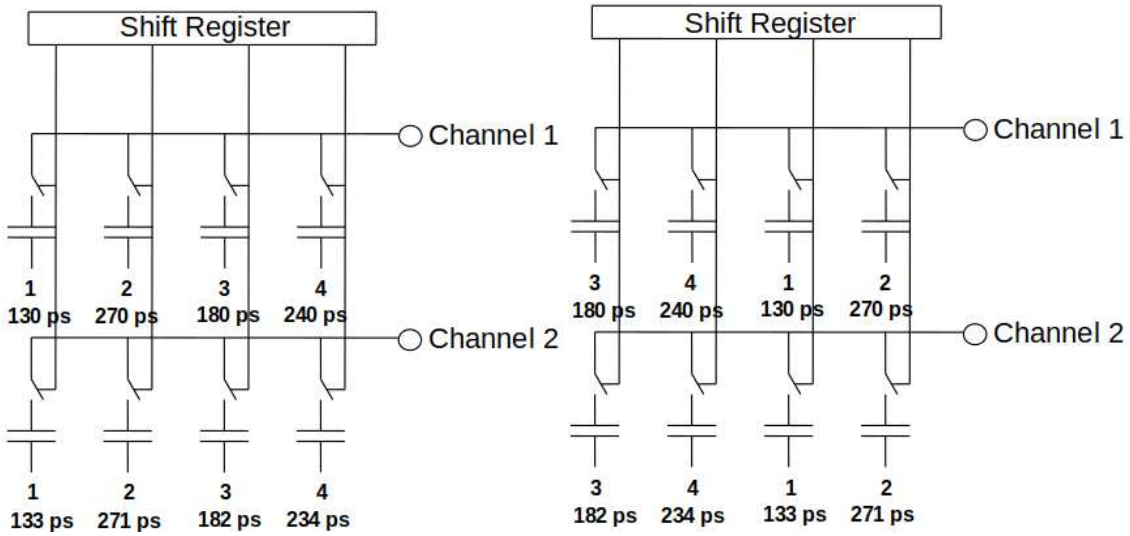
2.2.9 Cheap Calibration for Old DRS4 Evaluation Boards

The V5 already uses one NEW-TC from this work which increases its performance compared to older versions. If no budget is available to buy a V5, old versions of the DRS4 Evaluation Board can be recycled.

For example, the V3 can be calibrated with the 66 MHz clock signal provided by the board itself. For its realization the input resistors of the V3 have to be increased to 1 kΩ and the to be calibrated channel has to be connected to the 66 MHz clock of the DRS4 Evaluation Board as shown in fig. 2.15(a). After the calibration one should change the resistors back to maintain the dynamic range of the board. Alternatively, one can change the FPGA code and route the 66 MHz clock signal to the calibration channel. In that case only one channel can be calibrated. Thus, this TC outcome must also be applied to the other channels, which will cause a performance degradation of the DRS4-chip. In theory one can calibrate all iterations of the DRS4 Evaluation Board by using its dedicated 66 MHz clock. The results of the low budget solution for the V3 are available in fig. 3.24(c & d).

2.2.10 Calibrating Multiple Channels of an SCA

One has to calibrate all channels individually in order to get the best timing performance results. This sub-section will explain how to apply the NEW-TC to the individual channels. It is not trivial to use the just calibrated time information and apply it to multiple channels because another time-error occurs when an SCA is stopped. Since this is a systematical error, it does not have to be measured and there is an relative easy approach to solve this issue. When looking at fig. 2.12(a) one will find an example of an SCA with two channels each consisting of 4 cells and stopped at cell #1. Additionally a second c_{stop}-scenario is demonstrated for the same SCA in (b). Naively one would expect that both channels will stop at exactly the same time for both scenarios (c_{stop}=1 and c_{stop}=3). In reality they will be shifted a few pico-seconds in time. For example the voltage information in cell #1 of channel #1 could be stored 3 ps before being stored in cell #1 of channel #2. For cell #2 this permanent delay could be different, and so forth. Thus, every cell in a given



(a) scenario: c_{stop}= cell #1 **(b)** scenario: c_{stop}= cell #3

Figure 2.12: Example for two c_{stop} scenarios of the same SCA. Two calibrated channel of an SCA (n_{SCA}= 4) are shown. One can see that for channel #1, Δt_1 is 130 ps between cell #4 and cell #1. The $\Delta t_{x^*,x}$ between the same cells (x) of individual channels is unknown.

channel (x) has a measurable delay to its dedicated partner cell (x^*) of the other channels. Since it is a fixed delay one can define a global cell. If cell #4 would be the global cell, a delay of 0 ps is assumed to all other partner cells. In this example two channels are used, therefore there is only one partner cell.

$$\Delta t_{x^*,x} = \Delta t_{4,x}(\text{reference channel}) - \Delta t_{4^*,x^*}(\text{partner channel}) \tag{2.30}$$

(2.30) reflects the just introduced theory and can be applied to calculate the corrections for the 3 remaining delays. Thus, cell #3 in fig. 2.12(b) would get a correction factor of -6 ps ($180 + 270 + 130 - 182 - 271 - 133 = -6$). In other words, if this SCA stops at c_{stop}=3, channel #2 is always 6 ps earlier stopped compared to channel #1.

2.3 Voltage Calibration (VC) Methods for SCAs

A VC has to be executed for an SCA before proper usage. The resulting VC correction tables differentiate from chip to chip. The first VC-method which is introduced later (VC1) has the biggest impact for SCAs and should always be applied. Some

VC-methods depend on the c_{stop} because an SCA can be triggered to stop any time for the cell readout. Consequently, the c_{stop} has 1024 possibilities for the DRS4 case. In general, five corrections exist for SCAs. These corrections are the result of five VC-methods (VC1, VC2, VC3, VC4 and VC5). When applying all VC-methods, a voltage-corrected waveform results. This means in the DRS4 case that all 1024 cells digitize the correct voltages which fluctuate typically less than 1 mV (σ).

In the following five sub-sections the five VC-methods will be discussed further. Afterwards, one will find four VC realizations that are utilized in this work: The *Absence of VC-methods* (NO-VC), the *VC-method provided by the V3* (V3-VC), the *VC-method provided by CAEN* (CAEN-VC) and the *New VC-method developed in this thesis* (NEW-VC)

2.3.1 VC1: Individual Cell Offset Calibration

The digitized voltages of the stored waveform show different offsets for each cell. The main reason is that each sampling capacitor is read out by a separate buffer, which has a typical offset of 10-20 mV. These offsets can be measured by using an *Applied DC-Voltage for VCs of SCAs* (V_{cal}) and then subtracting these offsets in each measurement as an offset correction.

Alternatively one can connect the input to ground, which would be equivalent to V_{cal}= 0 V. Since the gain of an SCA is not linear, the first approach is favored. That means V_{cal} should be adjusted for VC1 according to the baseline level (DC-offset) of future measurements. Thus, performing VC1 not at the future baseline level will cause degraded timing results.

2.3.2 VC2: Time-Dependent Readout Offset Calibration

VC2 compensates for small supply voltage variations when a DRS4-chip is switching from sampling-mode to readout-mode. The different power consumptions of a DRS4 chip in these two modes cause a small dip in the power supply voltage, which cannot be recovered completely by the linear regulator or the blocking capacitors. The dip causes the DRS4 output to differ by several mV for a few µs after it has been stopped.

For the V3 this is only the case for the first channel, since the channels are read out one after the other. The X742 reads 8 DRS4 channels in parallel, so the VC2 has to be made for every channel.

2.3.3 VC3: Symmetrical Spike Calibration

The VC3 problem is understood and solved since May 2018[98]. The solution increases the readout time and is therefore not always applicable. Additionally, the VC3 is only used in the DRS4 and not necessarily required for other SCAs. If VC3 occurs, exactly four of the 1024 cells simultaneously show spikes in all channels of the DRS4-chip, which means that four sampled voltage values are increased by around 14 mV. The four spikes always appear in two spike-pairs. If one spike-pair is known the other is predictable. The cell-distance of one spike-pair to cell #512 is always the same as the other spike-pair to the same cell #512. If all clocks on the board are synchronized, the spikes will only appear for certain cells. In this case when the f_{SCA} is doubled, the possible regions of the spikes will be reduced by half. In the experiment described by Sitarek et al[73], the DRS4 chip shows a possible spike every 32^{nd} cell when sampling at a speed of 2 GSPS. Further, by stopping the DRS4-chip at 80 given cell positions, it is possible to reduce the spike problem to an acceptable minimum for this experimental setup.

Since the four spikes are located in all channels of the DRS4-chip at the same cell# positions, one free running channel can be used to apply the VC3 efficiently. The VC3 is relativity stable for all boards from PSI but fails for the X742. These VC3 failures are discussed in section 4.1.

2.3.4 VC4: Time Pedestal Calibration with Randomly Arriving Trigger

Some SCA-chips have the problem that residual imprints of the previously stored waveform distort the last sampled signal. This may cause the chip to respond differently to DC signals, AC signals or transient signals. In the case of the DRS3 chip, these so-called ghost pulses can cause a signal error up to 5 %, depending on

the sampling speed. This problem has been fixed for the DRS4-chip by issuing a clear cycle before a storage cell is written. Both sides of the storage capacitor are connected to ground by additional analog switches for a few nanoseconds before every write cycle, thus removing relatively efficiently any previous stored charge in the cell.

Still, when reading only a few cells of the DRS4-chip, there is a possibility that the read out cells behave differently compared to the other cells, due to an internal recovery process probably related to some internal heat-up. The recovery process follows an exponential behavior as described in Sitarek et al[73]. The MAGIC telescopes are using DRS chips as readout electronics. But only a few cells are read out. Thus, VC4 is mandatory for this experimental setup. In most cases, when all cells of the DRS4-chip are read in a row, the effect is negligible because cells usually have more than 1 ms to recover. However, the effect may influence single measurements and can cause outliers in a Gaussian distribution. VC4 is not performed for any measurement in this work. However, for a correct TC (section 2.2), it is recommended to discard these events. This can be accomplished by working with mean values and ignoring single events that are not inside a given acceptance region, e.g. $3\,\sigma$. In section 2.1.5 such a method is described. It is developed and utilized during this work for rejecting outliers while performing the TC-method.

2.3.5 VC5: Individual Cell Gain Calibration

Every cell has a not-linearly behaving gain which differs from cell to cell. The cell-to-cell gain spread causes level-dependent offsets up to 0.5 mV (see data sheet [99], Plot 2) and has a considerable effect on the time resolution. Therefore, in addition to VC1, each cell buffer has a slightly different gain, which can be measured by applying an additional DC voltage to the input. For instance one could apply an additional V_{cal}, e.g. 800 mV, to the input and measure the response of the cell. Increasing the number of V_{cal} for the VC5-calibration will improve the resulting correction function. The spectrum of V_{cal} should ideally cover equidistantly the whole dynamic input range.

Assuming a linear response function of each cell and correcting it with multiple

V_{cal} will result in an error of less than 1 % from the true measured voltage. The V3 follows the mentioned linear approach by applying V_{cal}=0 mV and also V_{cal}=800 mV in order to compute the linear gain for each individual cell.

The cell gain correction function should be evaluated in more detail to obtain the best results. Therefore, a multi V_{cal}-based cell-by-cell calibration of the non-linearity will further improve the DRS4 performance.

2.3.6 V3-VC (VC1, VC2, VC3 and VC5)

The V3-VC is identical to the *VC-method provided by the V5* (V5-VC). It can be understood from the provided C-code, which can be downloaded freely on the PSI web-page[100]. The following V3-VC is performed in all DRS4 Evaluation Boards. One can make the different VC effects visible, when running the DRS4 Evaluation Boards with their provided software as illustrated in fig. 2.13. Only VC4 is not performed and usually not necessary because all cells are read out when the DRS4-chip gets triggered.

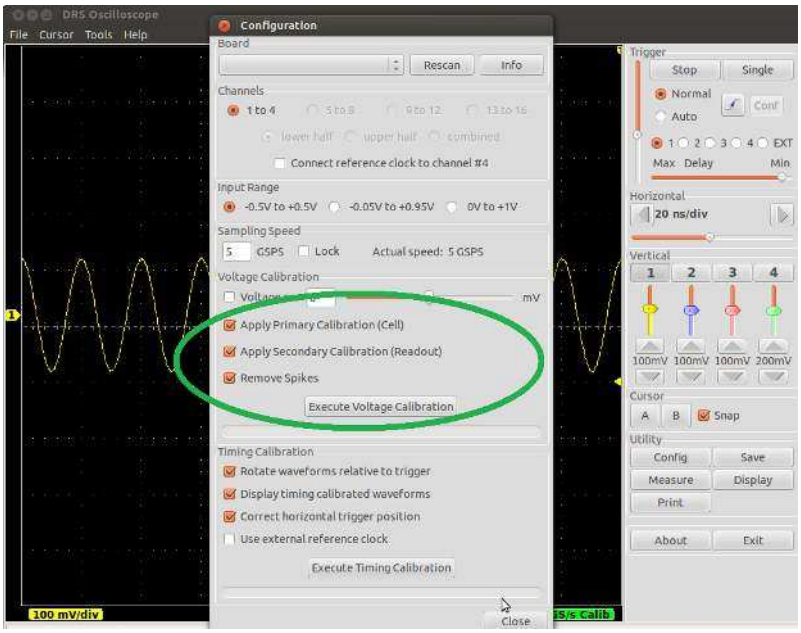


Figure 2.13: DRS4 Evaluation Board software showing three voltage correction options

In the C-code one can see that the calibration for VC1 and VC5 is performed first. For that purpose the four input channels get connected to ground, which means that all input cables have to be removed. The calibration for VC1 and VC5 is performed

independently from the c_{stop}. Since VC2 has a strong effect only on the first cells of the first channel, VC2 is not needed necessarily to perform the calibration of VC1 and VC5. Thus, the correlated error, that would be corrected by VC2, is almost canceled out by averaging over many c_{stop} positions. The VC1 information is used afterwards to perform the calibration for VC2. VC3 is performed by looking at a ninth channel of the DRS4 which is running with no input voltage. V3-VC is tested in more detail in section 3.1.

2.3.7 CAEN-VC (VC1, VC2 and VC3)

Identically to the CAEN-TC table, the CAEN-VC table is permanently stored in every X742 board inside the flash memory. That means before shipping the boards, the CAEN-VCs are individually calibrated in the CAEN facility. Considering that the electrical components including the DRS4-chip cannot age over time and the experimental conditions (e.g. temperature and humidity) are always the same, this would be the correct solution. Thus, improved measurement results will become available if the saved CAEN-VC in the flash memory is ignored and the just introduced VCs are performed manually when they are required.

The user manual from CAEN provides no information how the CAEN-VC is performed. In the software that comes with the board (C-code) one can see that VC1, VC2 and VC3 are available. VC3 is performed by checking all nine DRS4 channels for spikes. If all channels show a spike at the same cell position, it will be removed by subtracting the averaged voltage increase. However, the CAEN-VC does not work perfectly. Its test results are available in section 3.2.

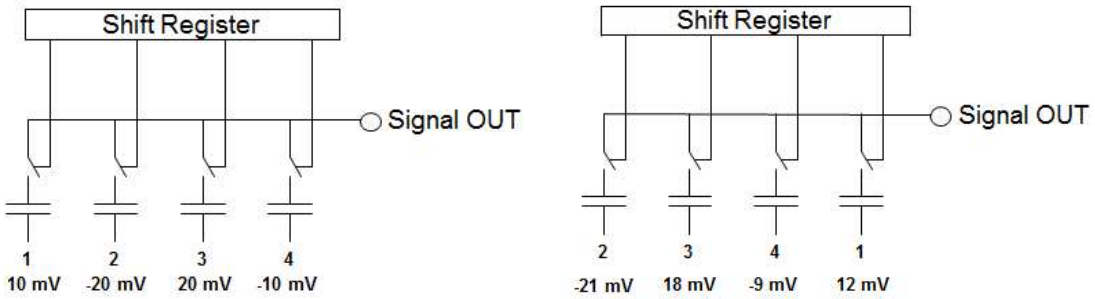
2.3.8 NEW-VC (Combining VC1 and VC2)

VC1 and VC2 are correlated. While VC1 is applied to the individual cell, VC2 only depends on the c_{stop}. The effect of VC2 is so small that it is usually ignored or considered to be canceled out when averaging many c_{stop} scenarios. The NEW-VC calibrates VC1 and VC2 simultaneously.

Fundamentally, every sampled voltage V_n of a cell consists of two sets of information. This information depends on the c_{stop} and can be written as:

$$\mathrm{VC1}_a + \mathrm{VC2}_b = V_n, \tag{2.31}$$

where $\mathrm{VC1}_a$ is the voltage offset VC1 (described in section 2.3.1) for the physical cell $\#a$ and $\mathrm{VC2}_b$ is the voltage offset VC2 (described in section 2.3.2) for the sampled cell $\#b$. a and b are restricted by the number of SCA cells. In the DRS4 case both variables are individually labeled from 0 to 1023. The n (in V_n) provides the number of equations and can be predicted. The minimum amount of equations is twice the number of SCA cells and increases linearly with the used c_{stop} positions. Thus, collecting waveforms exclusively from two c_{stop} positions is the minimum re-



(a) scenario: c_{stop}= cell $\#1$ **(b)** scenario: c_{stop}= cell $\#2$

Figure 2.14: Example for two SCA scenarios when the input channel is connected to ground. Illustrated are two c_{stop} scenarios of the same channel. The SCA-chip in this scenario consists of 4 cells. Thus, altogether four c_{stop} scenarios are possible: c_{stop}= cell $\#1$, cell $\#2$, cell $\#3$ or cell $\#4$.

quirement. More c_{stop} positions make the result more accurate, because noisy cell voltage measurements can be determined. In fig. 2.14 an SCA-chip consisting of four cells is given with two c_{stop} positions. By using (2.31) for the given example,

one will receive the following 8 linear equations:

$$\begin{aligned} VC1_1 + VC2_1 &= 10\,\text{mV} \\ VC1_2 + VC2_2 &= -20\,\text{mV} \\ &\vdots \\ VC1_4 + VC2_3 &= -9\,\text{mV} \\ VC1_1 + VC2_4 &= 12\,\text{mV} \end{aligned} \tag{2.32}$$

All systems of linear equations that yield from (2.31), like (2.32), are under-constrained and have therefore an infinite number of solutions. One has to define one of the unknown variables. Recommended is to define one of the $VC2_b$ to be 0 mV. In table 2.2 one will find an unique solution for such a case. Thus, for the DRS4 a system of at least 2048 linear equations have to be solved in order to compute VC1 and VC2. The NEW-VC is tested with the X742 (see section 3.4) and the V3 (see section 3.3).

Table 2.2: One possible solution for the example given in fig. 2.14 with $VC2_3 = 0$ mV.

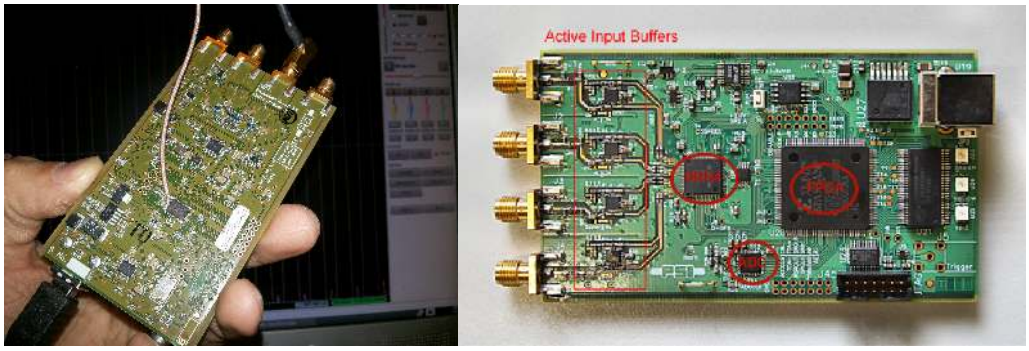
cell #	scenario a (mV)	scenario b (mV)	VC1 (mV)	VC2 (mV)
1	10	-21	13	-3
2	-20	18	-18	-2
3	20	-9	20	0
4	-10	12	-9	-1

2.4 Used Boards as Readout Electronics

In this section, all boards that are used in this work will be introduced with respect to time resolution (section 1.6). The best achievable time resolutions of these devices are evaluated in this work and summarized in table 3.12.

2.4.1 DRS4 Evaluation Board

In order to get used to the DRS4-chip, the PSI offers a DRS4 Evaluation Board. The software, which is necessary to run the board, is available as Open Source and can be downloaded on the PSI-webpage[100]. The software is written in C++ and runs on Windows, Linux and OSX. With an ordinary PC and an *Universal Serial Bus* (USB) cable it is relatively easy to get started. Thus, for many applications the DRS4 Evaluation Board can be used as a relatively cheap portable oscilloscope replacement. It typically costs around 1000 EUR.



(a) V3 back **(b)** V3 front

Figure 2.15: One can see that V3 fits in one hand. In (a) the internal 66 MHz clock is bypassed and connected to channel #3 to perform the NEW-TC.

There have been multiple iterations of the DRS4 Evaluation Board. Each iteration brought better software features and hardware improvements. The V3 is evaluated in detail in this work. The latest board, the V5, was designed because of the results of this doctoral thesis. The shipment started in March 2014. The V5 is highlighted by its convincing results and includes excellent time resolution as the new main feature. Additionally, the V5 is capable of triggering on every channel, which makes it easier for use in PET measurements, where two channels have to

trigger simultaneously. However, the V3 is mainly analyzed in this work and it is pictured in fig. 2.15. The V3 triggered the development of the NEW-TCs which can be found in section 2.2.

The DRS4-chip was designed in 2007 and has a bandwidth of 950 MHz. The sampling frequency ranges from 0.7 GSPS to 5 GSPS. The power consumption for the fastest f_{SCA} is around 40 mW per channel. The DRS4 contains 9 channels (N_{ch}) and the n_{SCA} is 1024 in each channel. Only 4 out of 9 channels are available for all DRS4 Evaluation Boards due to mechanical constraints of the connectors. Since the DRS4 is connected to a single 33 MHz ADC resulting in time steps (t_{clock}) of 30 ns, the dead time (t_{dead}) of the board can be calculated as:

$$t_{dead} = n_{SCA} \times N_{ch} \times t_{clock} = 1024 \times 4 \times 30\,\text{ns} \approx 0.123\,\text{ms} \tag{2.33}$$

The V3 channels have a 1 V dynamic range with an BW of 700 MHz. The SNR is equivalent to 11.5 bits. The fastest acquisition rate, which is restricted by the readout speed, is around 500 per second. The readout speed is limited by the USB port, which also delivers the voltage supply for the board. From t_{dead}= 0.123 ms, one can calculate that the maximal acquisition rate is $1/t_{dead} \approx 8000/\text{s}$ which corresponds to a data rate of around 15.5 Mbytes/s per channel. With an f_{SCA} of 5 GSPS, the digitized time in 1 second is $8000 \times 200\,\text{ps} \times 1024 \approx 1.6\,\text{ms}$. This is an event loss of more than 99.8 %. Thus, the low acquisition rate is the main drawback for this very fast and inexpensive ADC replacement.

Only the relevant features for this work have been named. More information about the DRS4 and SCAs in general are given in section 1.9.6. The utilized PSI calibrations for the DRS4-chip are available in section 2.3.6 and section 2.2.6. A complete documentation of V3, V5 or the DRS4 can be found on the web page of PSI[99].

2.4.2 CAEN Readout Electronics

Two broads the V1742 and the DT5742 are investigated. Both boards utilize the DRS4-chip and therefore similar performance is excepted compared to the V3. Both

will be referred to predominantly as the X742 in this work. In contrast to the V3, the X742 has only 3 f_{SCA} available (1, 2.5 and 5 GSPS). The selling price per channel of the X742 is around 2 times lower compared to the V3. The utilized CAEN calibrations for the DRS4-chip are available in section 2.3.7 and section 2.2.6.

2.4.3 Oscilloscope: Wave Runner 6050A and 640Zi

In general, oscilloscopes are capable to observe the change of electrical signals over time among parallel channels. In this work two modern digital oscilloscopes from Teledyne LeCroy are evaluated. Both oscilloscopes utilize fast flash ADCs and are far more expensive compared to the V3. Further, only the relevant parameters for timing will be named.

The *LeCroy WaveRunner 6050A Oscilloscope* (S5) settings for all performance test have been 500 MHz BW, 5 GSPS and 8 bits resolution. The DRS4 is superior compared to the S5 in all aspect of the specification. Thus, the V3 should also be superior in performance tests compared to the S5.

The *Teledyne LeCroy WaveRunner 640Zi Oscilloscope* (S20) was running with a BW of 4 GHz, 20 GSPS and a bit resolution of 8.5 bits artificially enhanced to around 11 bits. The S20 is used to evaluate the best achievable results among the boards. The S20 was additionally running with a BW of 1 GHz and a sampling speed of 5 GSPS which is close to the DRS4-chip parameters. Both manuals with more details are available on the web page of the company[101].

2.4.4 NIM Electronics

Three NIM Electronics boards with regards to time resolution have been tested [VIII]:

1st, the *Tenneelec Time-to-Amplitude Converter TC 861A* (NIM-TAC) will be named. The time resolution is 0.01 % of the full-scale plus 5 ps (FWHM). Thus, the best achievable time resolution with NIM-TAC is 10 ps (FWHM). The output voltage is analyzed with a 12 bit and a 14 bit ADC for the time resolution tests.

[VIII] The NIM Electronics specifications are defined by the norms EUR 4100 and AEC NIM (TIS20893).

Further specifications of NIM-TAC can be found in the manual[102], as well as more details about TAC in general in section 1.9.5.

2nd, tested is the *LeCroy Leading-Edge Discriminator 623B* (NIM-LED), which is an 8-channel LED. The output rise time of the NIM standard pulse is typically 2.1 ns with with a stability better than 0.1 %/°C[103]. Only the rise time and the noise is important for time resolution tests. Further details about LED in general can be found in section 1.9.1.

3rd, used is the *SIN Constant Fraction Discriminator 102* (NIM-CFD), which is a 6-channel CFD. A detailed description of CFDs can be found in section 1.9.2.

Additionally, three more modules of the NIM electronics are used to generate a TLL-trigger for coincident PET-events, which are the 3 channels of the NIM-LED, one module that continuously builds a sum of two channels and a NIM-to-TLL trigger converter. This is mandatory to trigger V3 and X742. It is also used to trigger the other boards guaranteeing that the experimental conditions are kept identical for all investigated boards. Fig. 2.16 illustrates its realization. The advantage of

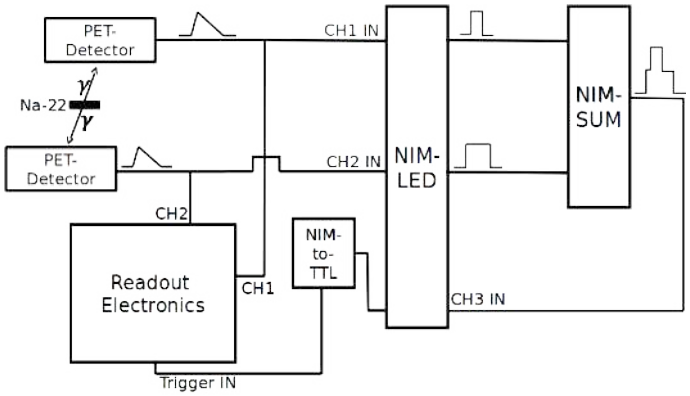


Figure 2.16: Schematic view of a trigger logic produced with the NIM electronics to trigger coincident PET-events. The time window is adjustable by modifying the length of NIM-LED output signal.

using an external trigger is to reduce the number of random events by providing a variable time window. Furthermore, by changing the TH values for the individual input channels of the NIM-LED, one can adjust the energy region of interest. Two channels of the NIM-LED are used for this purpose. When both channels produce an output signal (NIM-signal) inside a given time window, one can consider the two events to originate from the same β^+ decay. The time window is set by varying

the width of the two output signals of the NIM-LED. The two output signals are summed together and fed again to a third channel of the NIM-LED where the TH is set to 1 V. Thus, the third channel is only triggered when the sum of two NIM-signals are overlapping indicating a coincident PET-event. Finally, the NIM signal has to be converted to a *Transistor-Transistor Logic* (TTL) signal to trigger the tested boards, including the V3 and the X742.

2.5 Test Setups for Time Resolution Measurements

In the following 7 sub-sections one will find the test setup description for all performed experiments. They are divided in two categories. The first category uses ideal waveforms coming from a function generator. The first category is divided in the SP-test and the *Period Test* (P-test). Both methods enable the comparison of individual readout electronics.

Table 2.3: Summarized are all CRT-tests of this thesis. One can see that altogether seven PET-detectors are available and investigated in 11 CRT-tests (11 rows).

PET-detector	digitizer (TC)	crystal details	more details	results
APD+LSO	V3 (V3-TC)	$3 \times 3 \times 20\,\mathrm{mm}^3$	section 2.5.4	section 3.1.5
PET-INSERT	V3 (V3-TC)	15×15 crystals	section 2.5.4	section 3.1.6
SiPM+LSO	V3 (V3-TC)	$3 \times 3 \times 20\,\mathrm{mm}^3$	section 2.5.5	section 3.1.4
SiPM+LSO	X742 (NEW-TC)	$3 \times 3 \times 20\,\mathrm{mm}^3$	section 2.5.5	section 3.4.2
MPPC+PbWO	X742 (NEW-TC)	$1 \times 1 \times 5\,\mathrm{mm}^3$	section 2.5.5	section 3.4.3
reference PMT	X742 (NEW-TC)	3×3 crystals	section 2.5.5	section 3.4.2
reference PMT	X742 (NEW-TC)	3×3 crystals	section 2.5.5	section 3.4.3
PMT+LSO	V3 (V3-TC)	$3 \times 3 \times 20\,\mathrm{mm}^3$	section 2.5.6	section 3.1.3
PMT+LSO:Ca	X742 (CAEN-TC)	$5 \times 5 \times 5\,\mathrm{mm}^3$	section 2.5.6	section 3.2.3
PMT+LSO:Ca	X742 (NEW-TC)	$5 \times 5 \times 5\,\mathrm{mm}^3$	section 2.5.6	section 3.4.1
PMT+LSO:Ca	S20	$5 \times 5 \times 5\,\mathrm{mm}^3$	section 2.5.6	section 3.5.3

The second category provides the *CRT (FWHM) and* $\frac{\Delta E}{E}$ *of a PET-Detector Test* (CRT-test). For all CRT-tests a Na-22 source is placed between two PET-

detectors to capture coincident events. Except for one case (S20), all CRT-tests utilize the DRS4-chip as readout electronics. To guarantee coincident events for the DRS4-based readout electronics (V3 and X742) an external trigger is mandatory. The coincident events are accomplished with an external TTL-trigger of a NIM-electronic setup (see fig. 2.16). The signal width of the TTL-trigger must be longer than 30 ns to trigger the DRS4, because of the ADC readout speed of 33 MHz. Additionally, the PSI-suggested warming-up phase of 20 minutes is applied before measuring with the DRS4.

A CRT-test consists of the coincident (folded) time resolution measured in FWHM (CRT) and the $\frac{\Delta E}{E}$ of both involved PET-channels. To be specific, the CRT-tests are applied to PET-detectors consisting of different photodetectors. The CRT-tests are also evaluating different crystal-types with variating dimensions. It should be mentioned that one crystal-case is tested for all investigated photodetectors (APD, SiPM, PMT) for comparison reasons. For these CRT-tests a $3 \times 3 \times 20\,\mathrm{mm}^3$ LSO-crystal is used. The crystal is wrapped in 5 layers of white teflon tape and is coupled with a thin layer of optical grease to the active area of the photodetector surface. A summary of all performed CRT-tests is available in table 2.3. One can see that for most cases (except last row) the DRS4 is used as readout electronics utilizing either the NEW-TC or its dedicated board TC-method.

2.5.1 P-Test: Time Resolution for a Single Readout Channel

The P-test needs a function generator with an accurate adjustable period, ideally with low SNR and little time jitter. In this thesis the W2571[104] and the W3251[97] are used to generate periodic signals. In theory any kind of periodic waveform will work for the P-test like the saw-tooth waveform for example. However, sine waves show best time jitter behavior in general, which is also the case for the above mentioned function generators. Therefore, only sine waves are analyzed in this work. The fastest sine wave that can be produced by the W2571 is 240 MHz. The fastest sine wave of the W3251 is 100 MHz. The P-test originates from the NEW-TCs introduced in section 2.2 and delivers an easy technique to check whether the TC works correctly for an SCA-based board. Additionally one can check the time resolution

of other readout electronics like fast ADC-based boards. The idea behind the P-test is to calculate the time difference of repeating sine wave points resulting ideally in multiples of the period. The time information of a digitized sine wave can be obtained by utilizing (2.19) or (2.20). An example of a digitized sine wave is shown in fig. 2.9. In this work, the straightforward way of calculating the zero crossings using the double-sided correction described by (2.20) is performed for all P-tests. Hereby one has to pay attention in calculating the time between equally behaving edges of the signal. This means between two rising edges for example. This is because the time difference between a falling edge and a rising edge is not necessarily half the period as may be expected.

If a periodic signal is already used for the TC-method of the readout electronics, a different frequency should be used for the P-test. Also the new frequency should not be a multiple of the previous frequency.

One can think of two possibilities to illustrate the results of the P-test. The 1st possibility is to show all measured periods in one Gaussian distribution. Concrete, one would expect for a sine wave with a frequency of 100 MHz a Gaussian with a mean value of 10 ns. This would prove that the board time is calibrated correctly. The standard deviation would be an indication of the time resolution of the board.

The 2nd and more powerful possibility is to produce two plots from all measured Gaussian distributions. These plots summarize the P-test results of all 1st possibilities, thus all Gaussian distributions versus the delay. In practice, the first plot shows the time resolution (σ) vs. multiples of the period (delay). And the second plot would illustrate the offset from the expected delay vs. the delay.

Mainly the 2nd possibility of the P-test is utilized in this thesis. In rare cases the 1st possibility is additionally provided to provide the shape of some distributions. It must be noticed that the offset is calculated by subtracting the measured delay from the expected delay! This information is mandatory to understand the following TC results.

The P-test is the key method for analyzing TC-methods. The P-test is applied to three distinct f_{SCA} (5 GSPS, 2 GSPS and 1 GSPS) in combination with sine waves ranging from 30 MHz to 240 MHz. Additionally, all P-tests are performed with sine

waves consisting of a peak-to-peak value of 1 V. Further, the abbreviation "100 MHz P-test" refers to a measurement-performance provided in multiples of 10 ns-steps including the offset from the expected steps. Thus, a P-test frequency of 100 MHz results in approximately 20, 50 and 100 available delays for 5 GSPS, 2 GSPS and 1 GSPS respectively.

2.5.2 SP-Test: Time Resolution for Split Signal

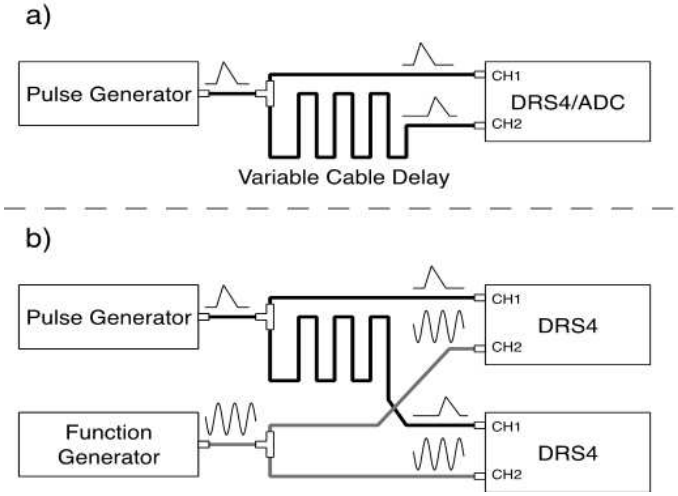


Figure 2.17: Layout of the split signal time measurements for two channels of one digitizer (a) and between two DRS4 Evaluation Boards (V3 or V5) synchronized by a sine wave (b). Figure taken from [31].

The actual time precision for the evaluated boards can be tested with the SP-test. Fig. 2.17(a) shows an illustration of the SP-test and in fig. 2.18 the picture of its realization.

In general, a short pulse is generated by a function generator or a pulser. Afterwards, the signal is split and the time difference between the arrivals of the two input signals is computed. The arrival time of one of the signals can be modified by applying a variable cable delay (fig. 2.18 shows a 10 m delay cable).

The P417 requires a 3 V coin-battery and therefore produces a low noise pulse. The positive pulse is characterized by a rise time around 3 ns and a total width of around 10 ns with a 1 V peak-to-peak value. The split pulse of the P417 is shown in fig. 2.19 and is digitized with a oscilloscope (S5). One can see by the height of the split pulse, that a hybrid power splitter is used (Mini-Circuit ZFSC-2-41) instead of

Figure 2.18: Shows a picture of a test setup for the SP-test. One can see that the pulse from the pulser is split via a power splitter. Additionally one split signal is delayed by around 50 ns before both are digitized in the V3.

a resistive splitter. For some boards an additional external trigger is mandatory and therefore a similar pulse compared to the P417-pulse is produced with a function generator. The W3251 is used for this task and provides an external trigger with an adjustable delay. The settings for W3251 can be found in table 2.4 and result in a pulse that is close to the P417-pulse with respect to peak hight, rise time, SNR and therefore to time resolution behavior.

With the mentioned pulse, the SP-test is performed by measuring multiple time differences between arriving split pulses for each cable delay. In most cases a digital LED (see section 2.1.1) is used to calculate the time resolution of the SP-test. A global TH of 300 mV is used for all SP-tests that perform a digital LED. Fig. 2.19 illustrates the TH value.

If both TH values are modified individually a 2D-matrix will result for the SP-test. The 2D-matrix shows the time resolution vs. all TH combinations. It should always show a coherent area in the middle region which indicate the best TH settings. Four examples of the 2D-matrix are available in fig. 3.47.

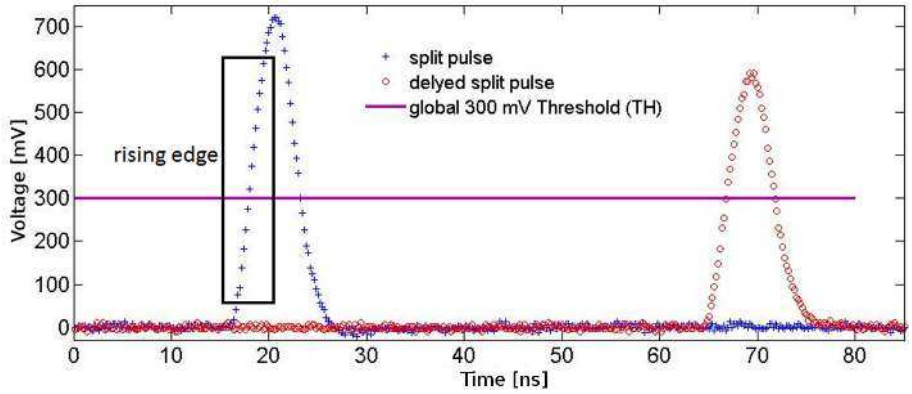


Figure 2.19: Split pulse digitized at 5 GSPS for the SP-test with S5 and a full range of around 1.1 V using 8 bits. The left signal height peaks around 720 mV and the delayed signal peaks at around 610 mV due to cable attenuation. The time difference between the signals is approximately 50 ns. The split pulse rise time is around 3 ns or 15 SPs. Figure taken from [31].

Table 2.4: W3251 settings to produce a standard pulse comparable to P417-pulse

option	value
waveform	pulse
voltage (peak-to-peak)	1 V
frequency	1.3 MHz
rise time	0.3 %
high time	0.0 %
fall time	0.0 %

The time resolution improves by using more points. Thus, the SP-test is also performed by fitting though 6 points of the rising edge with a digital LED.

Best results for the SP-test are achieved by cross-correlating[IX] (ICC or PCC) both channels. All non-baseline related SPs of the pulse are used in this case. Afterwards, a cross-correlation is performed. Typically 50 points of the split pulse are used per channel. In this case the first point is 10 SPs to the left of the given TH value of 300 mV. For the ICC 50 linear interpolations are made available for each channel to obtain equidistant SPs for all DRS4 waveforms.

Also tested is the time resolution (σ) between two independently running DRS4-

[IX] More details about the ICC and PCC can be found in section 2.1.4.

chips (fig. 2.17(b) shows an illustration). The trigger rate is preset below 1 Hz since the two independent running DRS4-based boards do not have a synchronized global trigger. The low trigger rate guarantees that all digitized waveforms of the first board belong to corresponding waveforms of the second board. The two-DRS4-chips experiment uses the digital LED for all time calculations. Also sampled is a split 100 MHz clock with a original peak-to-peak voltage of 3 V in two separate channels. The measured phase shift of the split clock is used to synchronize the two DRS4-chips. The given TH value for the 100 MHz clock is also 300 mV. Additionally, no baseline correction is performed for the 100 MHz clock. Note for all SP-tests in section 3.3.3, including the results of the two-DRS4-chips experiment, a different voltage compared to the provided value in table 2.4 is utilized. The utilized peak-to-peak voltage is increased to 1.35 V.

2.5.3 CRT-Test vs. Single Time Resolution (PET-Detector)

The CRT reflects the time resolution of a PET experiment. Thus, it provides the error in time of both involved PET-detectors. Therefore, a straight forward way to measure the time resolution of a single PET-detector is using two identical PET-detectors. The single or unfolded time resolution can be calculated by (1.14) and yields by dividing the CRT-test result by $\sqrt{2}$. This method is not an ideal solution since two PET-detectors cannot be build completely identical. Thus, one PET-detector will be treated better and the other worse than the true time resolution. Additionally one has to invest double to evaluate a single PET-detector.

Other than using two identical PET-detectors is by calibrating a single PET-detector once. This calibrated PET-detector functions as a reference PET-detector for future CRT-tests. The true time resolution of the tested PET-detector can now be computed by (1.14), which means subtracting the time resolution of the reference PET-detector from the CRT-test result and multiplying the outcome with $\sqrt{2}$.

In order to calibrate such a reference PET-detector two additional PET-detectors are required and ultimately one will calibrate three different PET-detectors. Thus three measurements (A, B and C) have to be performed which result in a system of

three equations when using (1.14) as

$$\begin{aligned}\sqrt{\sigma_{det1}^2 + \sigma_{det2}^2} &= \sigma_{\mathrm{A}} \\ \sqrt{\sigma_{det2}^2 + \sigma_{det3}^2} &= \sigma_{\mathrm{B}} \\ \sqrt{\sigma_{det3}^2 + \sigma_{det1}^2} &= \sigma_{\mathrm{C}}\end{aligned} \tag{2.34}$$

where $\sigma_{det1} \cdots \sigma_{det3}$ is the time resolution of the individual PET-detector and $\sigma_{\mathrm{A}} \cdots \sigma_{\mathrm{C}}$ the CRT of the three PET-measurements. Since all variables must be positive, there is a unique solution for (2.34) and the single time resolution of the reference PET-detector can be computed.

The first approach (two identical PET-detectors) is mainly utilized in this thesis for the CRT-tests. The alternative approach is applied once when analyzing multiple SiPM and crystal combinations. Further details about the mentioned CRT-test with SiPMs are available in section 2.5.5.

2.5.4 CRT-Test with APDs (PET-Detector)

The CRT-test with APDs is sub-divided in two categories. The first category investigates two facing detector-blocks of the PET-INSERT where a CRT of around 5 ns (FWHM) is expected. The PET-INSERT consists of 3×16 detector-blocks. Each block contains a 15×15 LSO crystal-matrix. The dimensions of a single LSO crystal are $1.5 \times 1.5 \times 10\,\mathrm{mm}^3$. The crystal-matrix is coupled to a Hamamatsu 3×3 channel APD 5054 array. The 9 APD channels are multiplexed to 4 channels. More details are available in the dissertation from Hossain [105].

The CRT-test for the mentioned PET-INSERT is performed with block #7 in coincidence with block #15 using a Na-22 source. The utilized readout electronics is the V3 when running with its dedicated TC-method (V3-TC). 50000 coincident waveforms from the PET-INSERT are digitized with the V3 running at 1 GSPS. 8 input channels are mandatory to perform a crystal-to-crystal CRT-test. Since the V3 offers only 4 input channels, a block-to-block CRT-test is measured with channel #2 and channel #4. The other two channels are not used. The measurement is repeated

inside a 3 T MRI-scanner. Three additional noise sources consisting of a 200 kHz, a 300 kHz and 500 kHz periodic signal are known from the gradient field. Among others, this study also triggered the installation of a filter to reduce the noise of the gradient system of the MRI device. The data are taken before the filter is installed, which has an impact on the CRT results.

For comparison reasons the second category of the CRT-test with APDs investigates a Hamamatsu $5 \times 5mm^2$-APD. It is a single channel version of the 9 channel array, which is used in the PET-INSERT. Also the corresponding integrated charge sensitive preamplifier from Siemens is used as a single channel version from Texas Instruments. The gain of the amplifier is $0.93\,\mu V/e^-$ with an RMS noise of $598 \pm 9.2\,e^-$ per pF (150 ns shaping time). A picture of the second category can be seen in fig. 2.20 where two identical PET-detector boards are aliened along a Na-22 source. One can see that a PET-detector consists of an APD coupled to a $3 \times 3 \times 20\,mm^3$

Figure 2.20: Shows a picture of the CRT-test with APDs coupled to a scintillator-crystal (second category).

LSO-crystal. The CRT-test is performed with the V3 running at 2 GSPS. The bias voltage is experimentally modified from 360 V to 410 V in 10 V steps. All APD voltage steps are globally applied to both APDs of the measurements. For each step the best time resolution is calculated. To calculate the time resolution for the best TH settings a digital LED (2 points) is used.

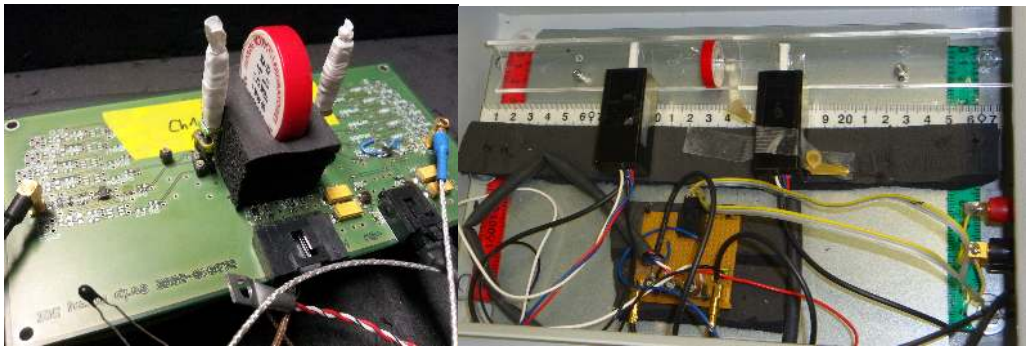
2.5.5 CRT-Test with SiPMs (PET-Detector)

The first SiPM measurement has been mentioned in section 1.10. In fig. 1.13(a) one will find a picture of this SiPM block. The detector-block (SiPM block) consists of

a 9 channel Hamamatsu MPPC-33-050C array coupled to 144 LSO-crystal-matrix. More information can be found in section 1.10. A detailed hardware-description of the SiPM block is published by Kolb et al[79]. To the mentioned SiPM block the Anger-logic is applied by digitizing all four V3-channels. However, since all 4 channels of the V3 were already occupied, an additional measurement with a single channel version of the mentioned SiPM block was performed. This additional measurement defines the CRT-test with SiPMs and consists of two identical PET-detectors (further referred to as SiPM1 & SiPM2). In particular the $3 \times 3mm^2$-Hamamatsu S10931 with a 50 μm pitch coupled to a $3 \times 3 \times 20\,\mathrm{mm}^3$ LSO-crystal builds one PET-detector (e.g. SiPM1). In fig. 2.21(a) the experiment is illustrated. The utilized amplifiers are the same as used for the SiPM block[79]. For comparison reasons, this CRT-test with SiPMs is performed with the DRS4 by applying the NEW-TC and the V3-TC.

In total, two CRT-tests with SiPMs have been performed in this work. One uses the abbreviation "SiPM" and the other the abbreviation "MPPC". The two abbreviations enable an easy distinction between both CRT-tests. The CRT-test with MPPCs (MPPC1, MPPC2 and MPPC3) is performed in combination with a reference PET-detector (see section 2.5.3). The reference PET-detector is a Hamamatsu PMT R9800 (reference PMT) coupled via optical grease to a $9 \times 9 \times 20\,\mathrm{mm}^3$ LSO-matrix. The matrix consists of nine $3 \times 3 \times 20\,\mathrm{mm}^3$ LSO-crystals wrapped in multiple layers of white teflon. The reference PMT voltage is set to -1200 V for all experiments. SiPM1 & SiPM2 from the first mentioned CRT-test together with the reference PMT result in three combinations, which are required to calibrate the reference PMT.

Unfortunately, when analyzing the data of the CRT-test with MPPCs, the reference PMT shows big variations every time it is moved. Also the calibration measurements, which were performed after all MPPC measurements had been completed, show an unpredictable single time resolutions between 300 ps and 600 ps (FWHM) for the reference PMT. Thus, most measurements cannot be compared with each other or other experiments with respect to time resolution. Yet, one of these 24 failed experiments is picked out because of its interesting results. It con-



(a) SiPM **(b)** PMT

Figure 2.21: Both figures show a picture of a CRT-test. In all cases the photodetectors are coupled to a single $3 \times 3 \times 20\,\mathrm{mm}^3$ LSO-crystal via optical grease. The crystals are wrapped in white teflon tape. In (a) two Hamamatsu S10931 SiPMs are shown and in (b) one can see two Hamamatsu R10560 PMTs aliened for detecting coincidence events of a Na-22 source.

cerns three CRT-tests with a *Lead Tungsten* ($PbWO_4$)-crystal in coincidence to the mentioned fluctuating reference PMT. In between these three CRT-tests the reference PMT was not moved. Additionally, one of the seven calibration measurements shows a similar photo-peak behavior for the reference PMT. Thus, the reference PMT can be calibrated roughly for the $PbWO_4$-scenarios. Further, the utilized $PbWO_4$-crystal dimensions are $1 \times 1 \times 5\,\mathrm{mm}^3$. Five crystal faces are polished and the exit face is diffuse. The crystal is wrapped in five layers of teflon. The active area of the utilized Hamamatsu MPPC is $1 \times 1\,\mathrm{mm}^2$ and coupled to the crystal through optical grease. The chosen micro cell sizes are $100\,\mu$m, $50\,\mu$m and $25\,\mu$m. As illustrated in table 1.1, $PbWO_4$ produces few scintillation-photons for PET events. On the other hand it has a short decay time. Therefore, the relative relation between the number of photons and the time resolution can be illustrated.

2.5.6 CRT-Test with PMTs (PET-Detector)

In total, two CRT-tests with PMTs can be found in this thesis, each with two identical PET-detectors[X]. For CRT-tests with PMTs, a digital LED (2 points) is mostly used and includes a walk correction unless otherwise specified.

The first PMT experiment utilizes LSO and the other PMT experiment uses

[X] Another CRT-test with a single PMT (reference PMT) is utilized in combination with SiPMs (details in section 2.5.5).

the faster LSO:Ca. For both PMT experiments no additional amplifier is used. In fig. 2.21(b) a picture of the first PMT experiment is shown. It consists of two Hamamatsu R10560 PMTs, each coupled via optical grease to a $3 \times 3 \times 20\,\mathrm{mm}^3$ LSO-crystal.

The second experiment uses two Hamamatsu H6780 PMTs coupled to $5 \times 5 \times 5\,\mathrm{mm}^3$ LSO:Ca crystals. Each PMT provides two output channels, the anode channel and the inverted 9 th dynode channel. As explained in section 1.8.1 the dynode channel provides the best timing and is therefore primarily evaluated. The optical connection between crystal and PMT consists of dedicated glue ($n \approx 1.5$) which hardens in ultra-violet light. Therefore, this experimental test setup can be re-used with constant performance results. This is not the case if the optical connection consists of an aging optical grease (first experiment).

Chapter 3

Results

The results of the previous introduced readout electronics (see section 2.4) with respect to time resolution are presented in this chapter and grouped in 5 sections. In the first two sections the results of the DRS4-boards are shown when applying their old TC-methods (CAEN-TC and V3-TC). After that the results of the DRS4-boards are shown with all new calibrations. This includes DRS4-chip results for different temperature conditions, sampling frequencies and long run-time. Finally, one will find the results of other readout electronics utilizing the same measurements as performed previously with the DRS4-based boards.

One has to separate all results between artificial signals (P-test and SP-test) and real PET-data (CRT-test). Details concerning the mentioned tests are provided in section 2.5.

3.1 V3 when Utilizing its Dedicated Calibrations

Before the time resolution results are illustrated, some general V3 results are summarized including the baseline noise results.

The maximum acquisition rate of the V3 is reached at around 500/s. The trigger rate has to be greater than 1000 Hz to constantly reach this acquisition rate. The V3 electronics is designed to trigger the DRS4-chip anytime, thus all 1024 c_{stop} are available. The trigger delay is adjustable from 26 ns up to 1.3 μs. The measured probability of a double spike-pair (described in section 2.3.3) is around 20 %. The

location of the double spike-pair is decoupled from c_{stop} and therefore unpredictable.

If the V3-VC is switched off, the baseline noise across all sampling frequencies is around 8 mV (RMS). The baseline noise always result in a Gaussian distribution when applying the V3-VC. One million digitized baselines resulted in an averaged DC-offset of around 0.41 mV with a fluctuation of around 0.12 mV (σ). When histogramming the 1024 SPs of an individual baseline, its baseline noise is 0.37 mV (σ). A non-linearity around 1 mV over the dynamic range is measured for a rectangular input signal ($\pm$200 mV). More precise non-linearity measurements are demonstrated in Yang et al[106].

However, when looking at individual baseline noises of the 1024 cells, one can measure roughly $\pm$5 cells with increased cell noise, surrounding a center cell, which is cell # 1016 at 5.12 GSPS. 10 k baseline events are measured to investigate the noise

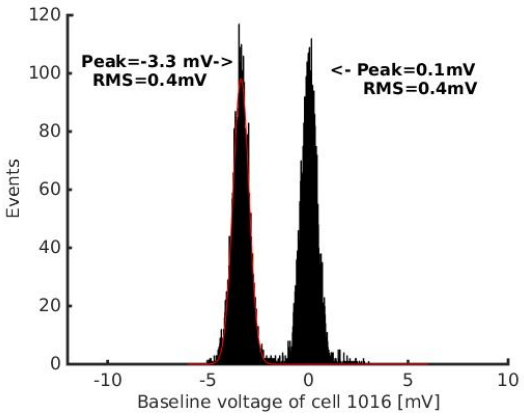


Figure 3.1: Two-state-effect of the V3 for cell # 1016 (channel # 1) when sampling at 5.12 GSPS.

increase of cell # 1016 (center cell). The measurements are taken from channel # 1 of the V3 when sampling at 5.12 GSPS. The measurement results are histogrammed in fig. 3.1. The histogram shows a 50% chance that the cell baseline is shifted 3.4 mV resulting in two distinguishable states. Each state shows a baseline fluctuation of around 0.4 mV which is consistent with the typical DRS4 baseline noise. The surrounding cells show a similar two state behavior, but with less shift. This two-state-effect becomes weaker the further away the individual cell is from the center cell. After $\pm$3 cells, the two separated Gaussians fuse together to a single Gaussian with increased noise behavior. After $\pm$6 cells the effect gets negligible. The effect

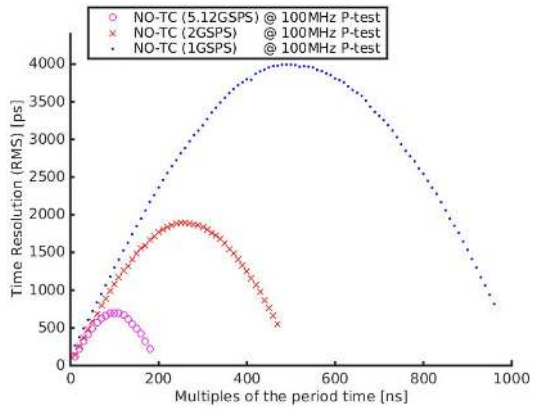
also decreases further away from channel # 1. Thus, channel # 9 has the least noise in this region. The center cell position depends on f_{SCA}. For 2 GSPS the center cell is cell # 1011 and at 1 GSPS the strongest noise behavior comes from cell # 1010. It should be mentioned that the two-state-effect influences the preset sampling speed of the DRS4-chip. The results of this effect are available in table 3.6.

The next 6 sub-sections summarize the results of the test setups (see section 2.5) before the NEW-TC was developed. However, the following results triggered the new development and underline the importance of a reliable time calibration.

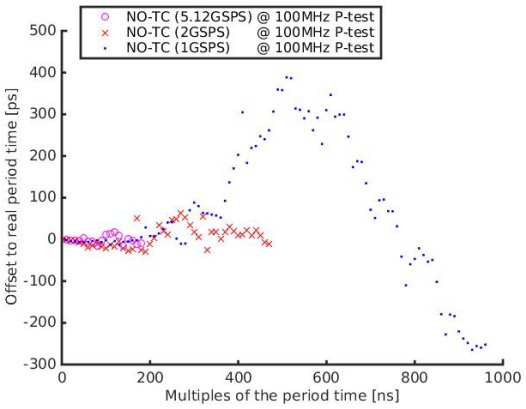
3.1.1 P-Test

The 100 MHz P-test results for NO-TC can be found in fig. 3.2. One can see that the V3 is tested for the sampling speeds 5.12 GSPS, 2 GSPS and 1 GSPS. Fig. 3.2(a) shows the time resolution (RMS) vs. the delay. One can see that the worst time resolutions (RMS) are always at $\frac{T_{SCA}}{2}$, which is around 0.7 ns (5.12 GSPS), 1.9 ns (2 GSPS) and 4 ns (1 GSPS). Independent from the sampling speeds the best time resolution (RMS) is around 120 ps which is only measured for very short or very long delays. Fig. 3.2(b) illustrates the corresponding offset vs. the delay. One can see that the 5.12 GSPS case has a maximum offset of 20 ps and the 1 GSPS case varies up to 400 ps from the true delay. Four example distributions of this P-test are provided in fig. 3.2(c - f). (c) shows all the time measurements of the first period and (d) illustrates the time resolution of ten periods when sampling at 5.12 GSPS. (e) shows the time resolution of all 26^{th} period calculations (2 GSPS) and (f) presents the time resolution of all 54^{th} period measurements (1 GSPS). The histogram examples cannot be measured with a Gaussian fit as visible in fig. 3.2(d - f). Therefore, it is replaced by the RMS value which is calculated with (1.11). The P-test histogram with the largest RMS value of 4 ns and a maximum spread of around 12 ns is shown in fig. 3.2(d). Additionally, the histogram peaks at both edges which causes the worst case scenario for this RMS calculation. Most 1 GSPS cases have a spread of around 12 ns but the peaks are less spread, which in turn results in improved RMS values.

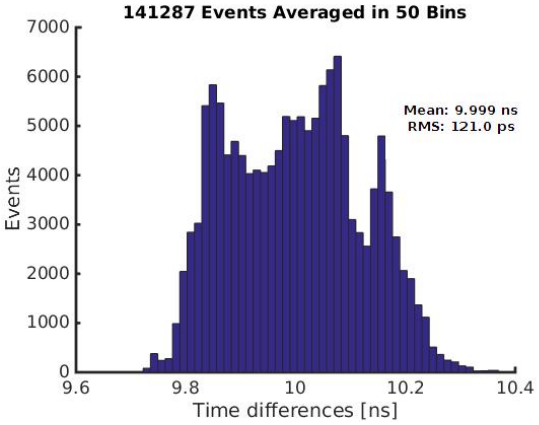
The previous P-test is repeated with the V3-TC being switched on. The result



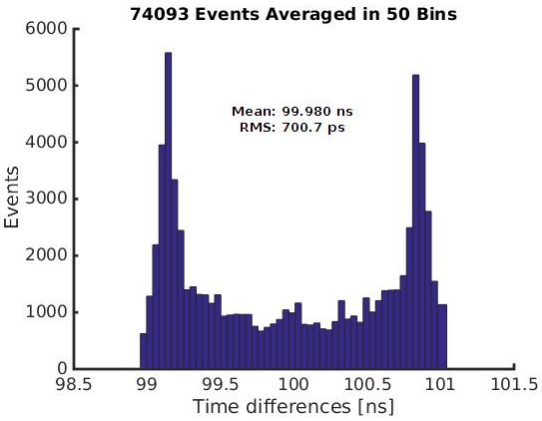
(a) RMS values of P-test



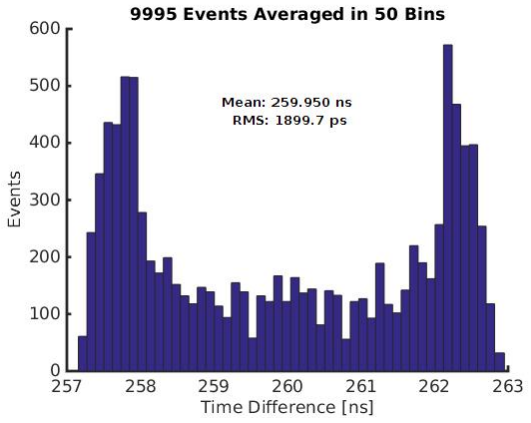
(b) Offset of P-test



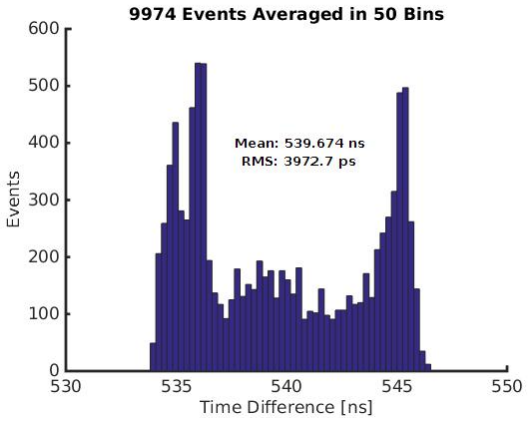
(c) P-test expecting 10 ns



(d) P-test expecting 100 ns

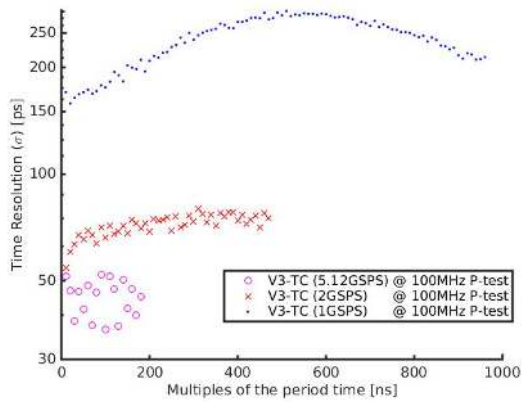


(e) P-test expecting 260 ns

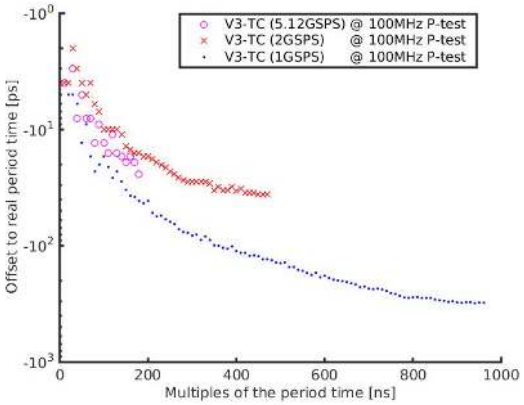


(f) P-test expecting 540 ns

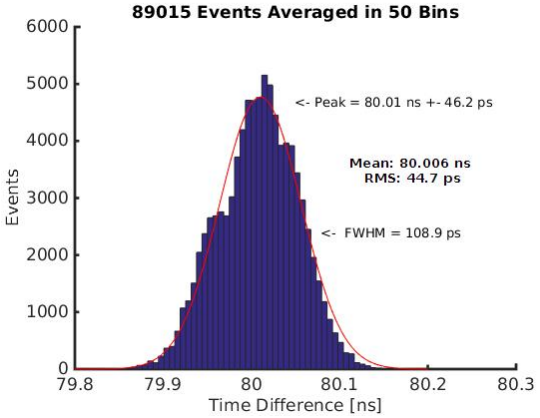
Figure 3.2: 100 MHz P-test utilizing the V3 (NO-TC). (a) shows the time resolution (RMS) vs. the delay and in (b) one will find its corresponding offset. Four corresponding distributions of this P-test are illustrated in (c - f). The DRS4 is running at 5.12 GSPS (c & d), 2 GSPS (e) and 1 GSPS (f).



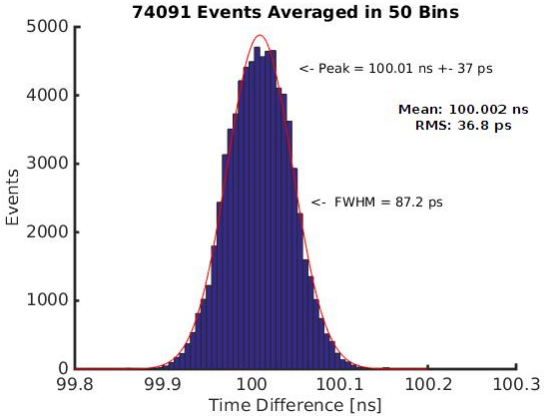
(a) σ values of P-test



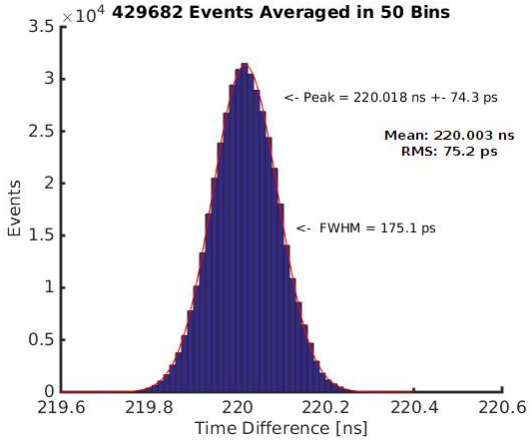
(b) Offset of P-test



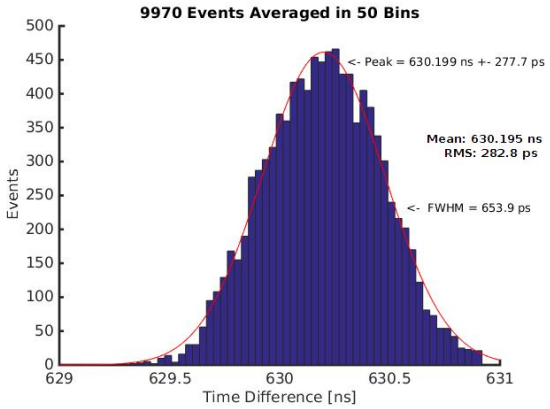
(c) P-test expecting 80 ns



(d) P-test expecting 100 ns



(e) P-test expecting 220 ns



(f) P-test expecting 630 ns

Figure 3.3: P-test with a 100 MHz sine wave for the V3 when utilizing the V3-TC. Both plots (a & b) use a logarithmic scale for the y-axes. (a) shows the time resolution (RMS) vs. the delay and in (b) one will find its corresponding offset. The DRS4 is running at 5.12 GSPS for the histograms in (c & d), at 2 GSPS for (e) and at 1 GSPS for (f).

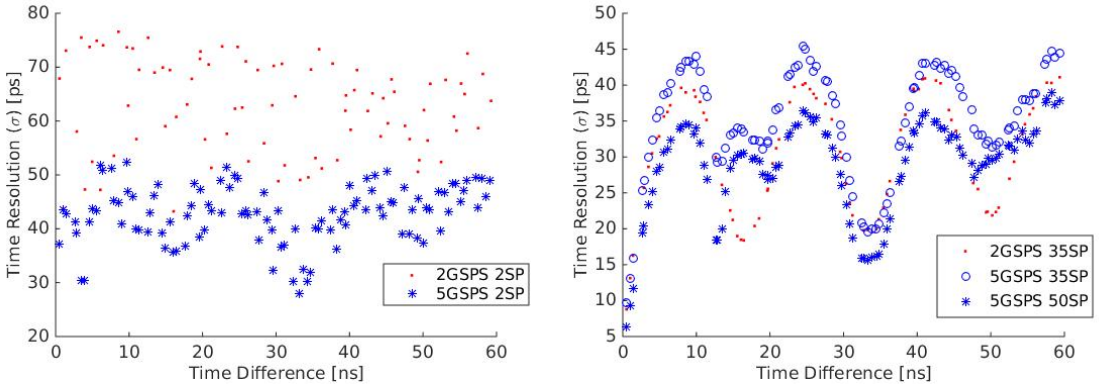
of this P-test can be found in fig. 3.3. Consequently, fig. 3.3(a) provides the time resolution (σ) vs. the delay and (b) displays the corresponding offset vs. the delay. The time resolution of the 1 GSPS case is between 200 ps and 300 ps (σ) with an offset up to 300 ps. On the other hand the time resolution for the fastest sampling speed (5.12 GSPS) oscillates between ≈35 ps and ≈50 ps (σ) with an offset peaking at 20 ps. Additionally, illustrated in fig. 3.3(c - f) are four distributions of this P-test. Some 5.12 GSPS distributions do not show a perfect Gaussian behavior like fig. 3.3(c) which shows time measurements of the eighth period. In contrast fig. 3.3(d) results in a Gaussian distribution for the time resolution of ten periods. Altogether around 30% of all distributions look similar to fig. 3.3(c) or worse when sampling at 5.12 GHz, which means that the Gaussian shape is missing. Fig. 3.3(e) shows the 22$^{\text{nd}}$ period histogram (2 GSPS) and the 1 GSPS-example in fig. 3.3(f) presents the timing histogram of the 63$^{\text{rd}}$ periods. All 150 histograms of these two sampling speeds look similar coming close to Gaussian distributions.

3.1.2 SP-Test

The precision of the V3-TC applied to the V3 (5.12 GSPS and 2 GSPS) will be shown in this sub-section with the SP-test (see SP-test explanation in section 2.5.2). The utilized algorithms for the SP-test are the digital LED and the PCC. Both methods are applied to the same dataset of waveforms. The results of these methods are presented in fig. 3.4. Both plots (a & b) show the time resolution (σ) vs. the time differences of the cable delay. Fig. 3.4(a) visualizes the results of the digital LED. The digital LED calculates the time at the given TH of 300 mV using only 2 SPs. The time resolution for the 2 GSPS case varies between 43 ps and 78 ps (σ) without any distinct pattern. An improvement was detectable for the 5.12 GSPS case with values between 27 ps and 52 ps (σ).

Fig. 3.4(b) illustrates the results of the PCC with more than 30 SPs. Two different cases for the PCC are investigated when sampling at 5.12 GHz. The first case uses 35 SPs and the other 50 SPs. The start SP of the PCC is 10 SPs and 5 SPs left of the given TH for 5.12 GSPS and 2 GSPS respectively. Four templates have been produced for the PCC, one for each sampling speed and channel. Each template is

computed out of 1 million events. One can see in fig. 3.4(b) that the time resolution



(a) SP-test with digital LED **(b)** SP-test with PCC

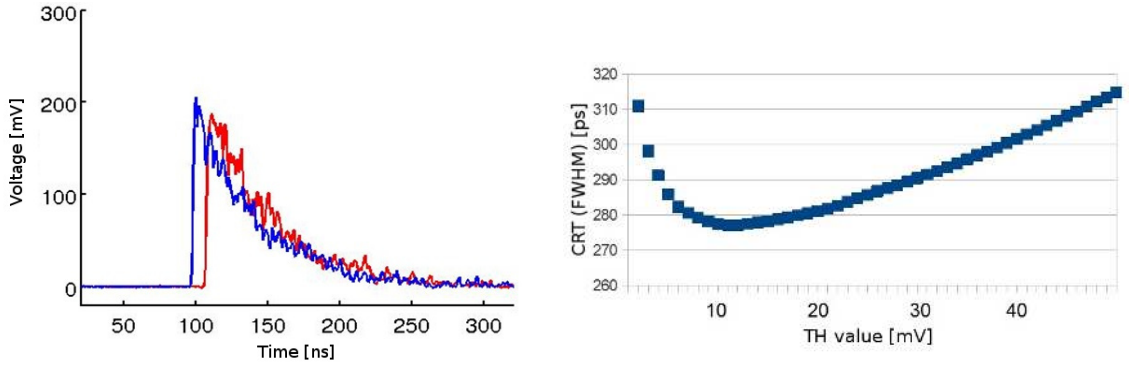
Figure 3.4: SP-test for the V3 when utilizing the V3-TC while sampling at 5.12 GHz and 2 GHz. Both plots (a & b) show the time resolution (σ) vs. the delay, but for two different analyzing techniques.

follows a sine wave pattern when the delay increases. The 2 GSPS PCC improves the time resolution between 20 ps and 40 ps (σ). More SPs cause a better time resolution in the 5.12 GSPS PCC case and results in a standard deviation between 15 ps and 35 ps for delays greater 2 ns. For short delays (smaller 1 ns) the time resolution is dramatically improved to around 5 ps compared to the digital LED with 37 ps for the same delay. Interestingly, all three PCC curves indicate a 60 MHz sine wave.

3.1.3 CRT-Test with PMTs Coupled to LSO

The first CRT-test of this work is summarized in this sub-section. Two identical PET-detectors are investigated consisting of a PMT coupled to LSO. Further experiment details are available in section 2.5.6 (keyword: first experiment).

The CRT-test in fig. 3.5 utilizes the V3 (V3-TC) when running at 2 GSPS. Both channels of a coincident PET-event are displayed in fig. 3.5(a) and each channel illustrates one analog output of a PMT. The rise times of both channels are in the region of 3-4 ns. The amplitudes of the photo-peak are around 190 mV for both channels. The delay between PMT #1 and PMT #2 is 180 cm or around 9 ns. Fig. 3.5(b) illustrates the CRT-test result (2-points LED). The TH values are changed globally, since the photo-peak energies of both channels are equal. The best results are

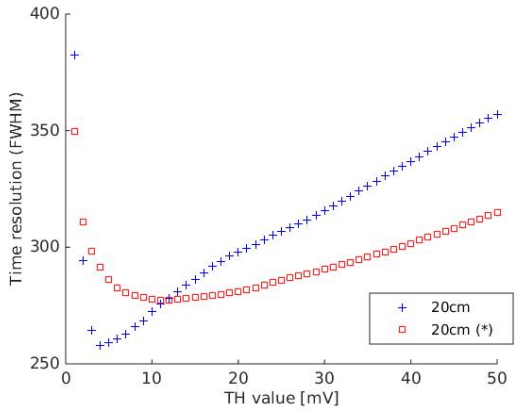


(a) Digitized PMT channels **(b)** Time resolution vs. global TH

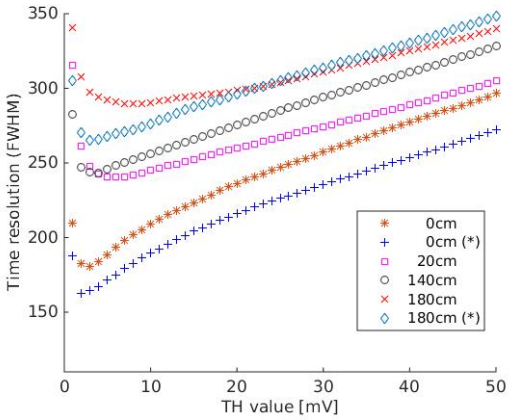
Figure 3.5: CRT-test with PMTs (b) and a dedicated single event (a) when utilizing the V3 (V3-TC) at 2 GSPS with a delay of 180 cm.

achieved with a global TH to 12 mV which is around 6 % of the photo-peak. With this settings the CRT is 276 ps (FWHM). Further, no walk correction is performed and all coincident events are used with energies inside the photo-peak. Fig. 1.2(b) illustrates the Na-22 spectrum of channel #1. The energies in this spectrum are calculated by integrating over the complete waveforms. The resulting $\frac{\Delta E}{E}$ of this spectrum is 10.5 %. The $\frac{\Delta E}{E}$ of channel #2 is 10.9 %.

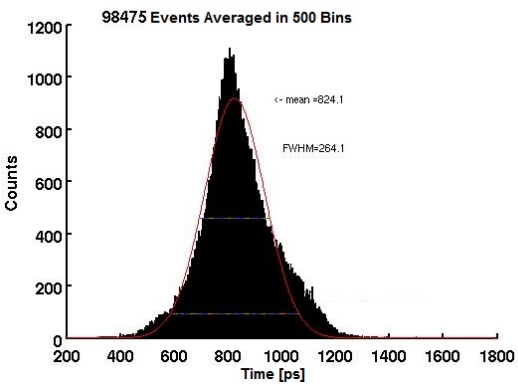
The measurement in fig. 3.5 was repeated the following day and resulted in a similar outcome. As expected the CRT slightly degrades which is caused by the drying of the optical grease. Its curve can be found in fig. 3.6(b) labeled with "180 cm". Other cable delays are investigated additionally for this CTR-test. These measurements are triggered because fluctuating CRT results have been measured in the previous section 3.1.2 when changing the cable delay. The label indicates the cable delay between both PMT channels. The input channels of the V3 are interconverted for the labels with the additional naming " (*) ". Four different cable delays have been analyzed in all. Three out of four cable delays are interconverted which results in inconsistency in terms of CRT behavior. In fig. 3.6(a) the CRT-test results with a digital LED for two delay cases are found when sampling at 5.12 GSPS. One can see that the CRT varies more than 20 ps. Further, also the best TH positions differ although only the input channels have been swapped around. In fig. 3.6(b) the results for different cable delays are found when running at 2 GSPS. A similar behavior is investigated for the 5.12 GSPS case. Additionally, a short delay results



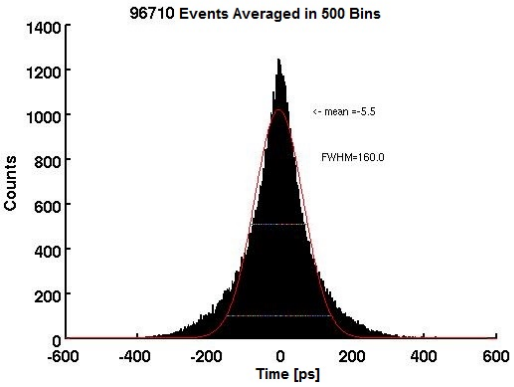
(a) Digital LED for 5.12 GSPS



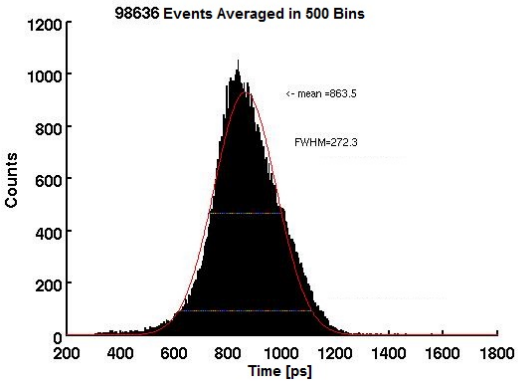
(b) Digital LED for 2 GSPS



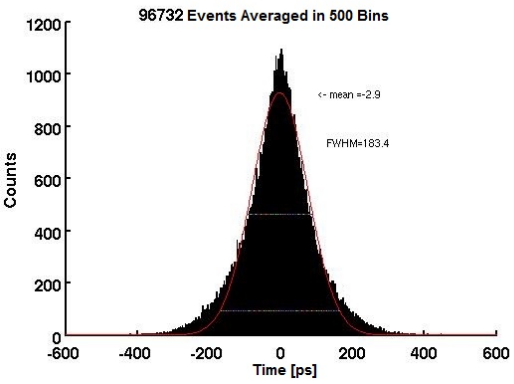
(c) 5.12 GSPS, 20 cm delay, TH=3 mV



(d) 2 GSPS, 0 cm(*) delay, TH=3 mV

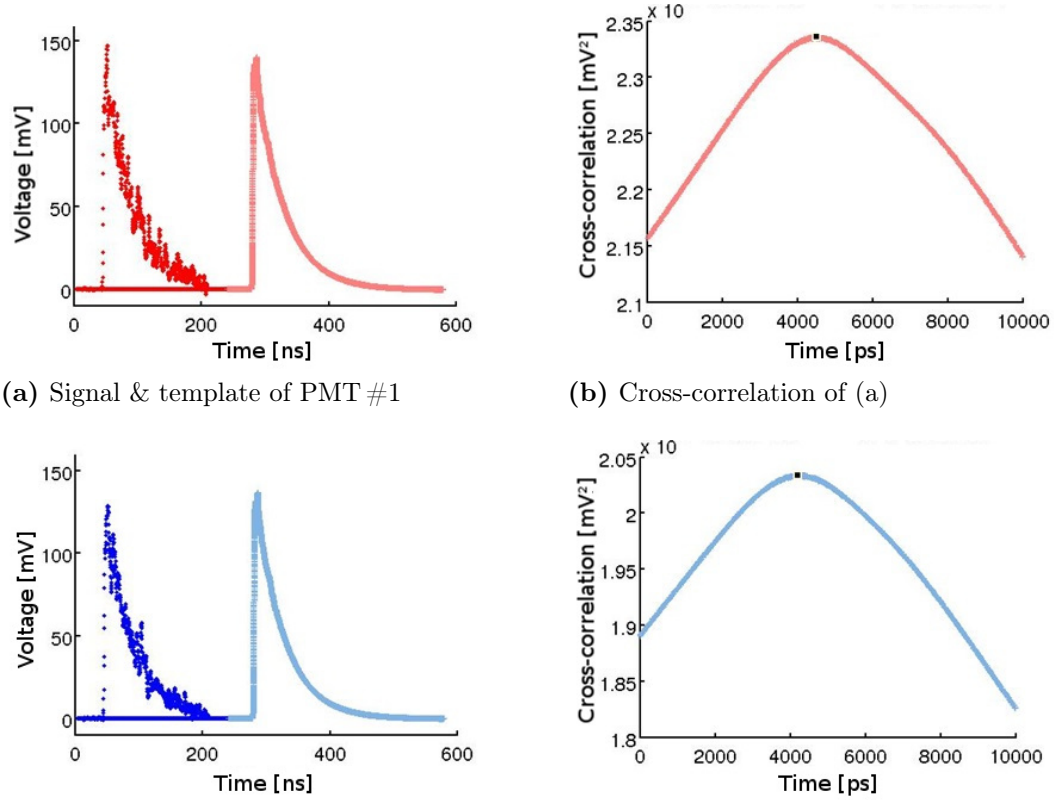


(e) 5.12 GSPS, 20 cm delay, TH=10 mV



(f) 2 GSPS, 0 cm(*) delay, TH=10 mV

Figure 3.6: CRT-tests with PMTs (a & b) and their dedicated histograms (c - f) when utilizing the V3 together with the V3-TC. The cable delay between both PMTs is provided in cm. For delays labeled with " (*) ", the PMT cables have been switched.



(a) Signal & template of PMT #1

(b) Cross-correlation of (a)

(c) Signal & template of PMT #2

(d) Cross-correlation of (c)

Figure 3.7: Single CRT-test event with PMTs when using the PCC with the V3 (V3-TC).

in a better CRT and the overall fluctuation ranges from 160 ps to 290 ps (FWHM). The histograms in fig. 3.6(c-f) are four examples of best CRTs from the curves in fig. 3.6(a & b) . For instance, the CRT result in fig. 3.6(c) represents the lowest point (160 ps) of the curve in fig. 3.6(a) which is labeled with 18 cm. One can see that none of the four histograms results in a Gaussian distribution. This is also the case for 90 % of the other histograms which are not illustrated.

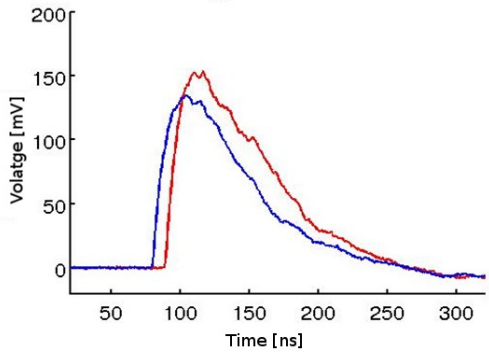
Additionally, the PCC (described in section 2.1.4) was performed for three different delays (0 cm, 20 cm and 180 cm). For this reason 1 million events have been collected for each channel to compute a template. Various PCC-setting have been tested additionally to achieve the best CRT. All sampling speeds have been investigated, although the best results are expected for the fasted sampling speed. The whole waveform is cross-correlated in the first computation in order to use all information that is stored in the waveform. Fig. 3.7(a) shows the modified signal of

channel #1 and its template with an amplitude of around 145 mV. In fig. 3.7(b) one can see the corresponding cross-correlation of (a). Fig. 3.7(c) shows the modified signal of channel #2 and its template with an amplitude of around 140 mV. Consequently, fig. 3.7(d) illustrates the cross-correlation example of (c). A single time difference is calculated by subtracting the measured times of the high points from (b) and (d), which is symbolized by a black dot in the corresponding curve. By repeating this procedure, 10 k time differences for each PCC-adjustment are computed and the resulting CRT is calculated. After optimizing the parameters, the best results are achieved when sampling at 5.12 GSPS with a modified signal length of 15 ns (65 SPs). The best CRT outcome of the PCC is around 360 ps (FWHM). It is independent of the delay and all results showed a perfect Gaussian distribution. Interestingly the results did not change if only the energies inside the photo-peak are accepted or all energies are allowed for the PCC.

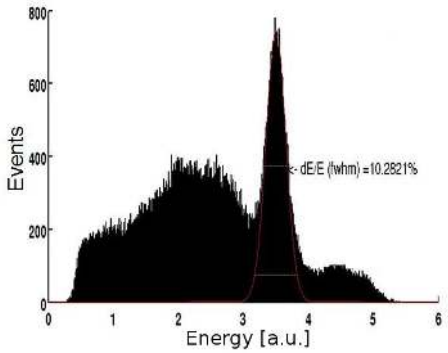
3.1.4 CRT-Test with SiPMs Coupled to LSO

Fig. 1.13(b) shows the first experiences of SiPMs in combination with the V3 in this work. To be specific, a flood histogram of a SiPM block is computed by utilizing the 4 channels of the V3. As a result all 144 LSO-crystal positions are better distinguishable compared to the readout electronics used by Kolb et al[79].

The CRT-test in this sub-section is performed with a one-to-one coupled modification of the mentioned SiPM block. All details about the experiment are provided in section 2.5.5. Fig. 3.8(a) shows both channels of the coincident PET-event digitized with the V3 (V3-TC) running at 2 GSPS. Each channel illustrates the analog output of a SiPM coupled to LSO. The rise time of both SiPM-detectors is around 15 ns. In fig. 3.8(b) one will find the Na-22 spectrum of SiPM1 resulting in $\frac{\Delta E}{E}$ of around 10.3 %. The SiPM output is not energy corrected for non-linearity. Thus, the true $\frac{\Delta E}{E}$ will be more in the region of 13 %. SiPM2 shows a similar $\frac{\Delta E}{E}$. The amplitudes of the photo-peak are around 185 mV for both SiPM-detectors. Therefore the same TH value is used globally in both channels. The best CRT when performing the digital LED is achieved with a TH value of 4 mV, which is around 2 % of the photo-peak. No walk correction is performed. Additionally, all coinci-



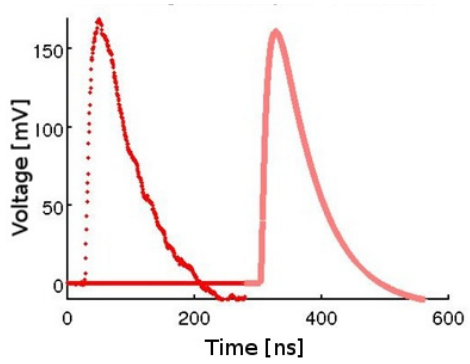
(a) Coincident event of SiPM1 and SiPM2



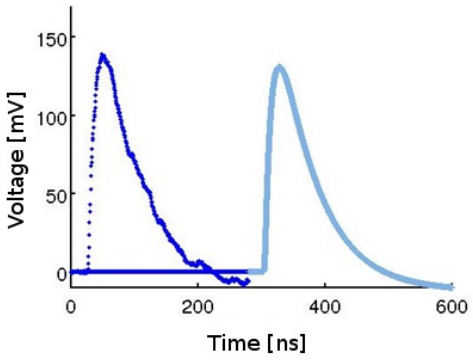
(b) Na-22 spectrum of SiPM1

Figure 3.8: Single event of the CRT-test with SiPMs coupled to LSO and a Na-22 spectrum digitized with the V3.

dent events with energies inside the photo-peak have been utilized. The CRT is 572 ps (FWHM) with these settings. Unlike in the previous section 3.1.3 all time measurements showed a Gaussian distribution.



(a) Signal & template of SiPM1



(b) Signal & template of SiPM2

Figure 3.9: Single coincident SiPM event for the PCC with the V3 (V3-TC) running at 2 GSPS.

Similar to section 3.1.3, the PCC (described in section 2.1.4) is additionally applied to the CRT-test with SiPMs. For this reason 1 million events are collected for each channel to compute a template. The DRS4 is running at 2 GSPS to capture the full waveform. The whole waveform is cross-correlated in the first computation to lose no information. However, best results are achieved when 50 ns (100 SPs) are cross-correlated with the template. In fig. 3.9 one will find a PCC event for both SiPM-channels. Shown are the modified signals of SiPM1 and SiPM2 together with their dedicated templates. The amplitudes of the templates lie around 150 mV.

The best CRT result of the PCC is 719 ps (FWHM). Identical to the results in section 3.1.3, no timing improvement is observed if only the energies inside the photo-peak are accepted or the Compton continuum is included for the PCC.

3.1.5 CRT-Test with APDs Coupled to LSO

The CRT-test results of the Hamamatsu APD coupled to LSO will be presented in the following pages. More details about the CRT-test with APDs are given in section 2.5.4. Also a picture of the experimental setup is available in fig. 2.20.

First the preamplifier from Texas Instruments was tested. Test pulses with a rise time of 12 ns were amplified to pulses with a rise times of 13.4 ns with this amplifier. Afterwards the CTR-test is performed with the V3 (V3-TC). Fig. 3.10 shows an example of the analog outputs of both APD channels coupled to LSO. One can see

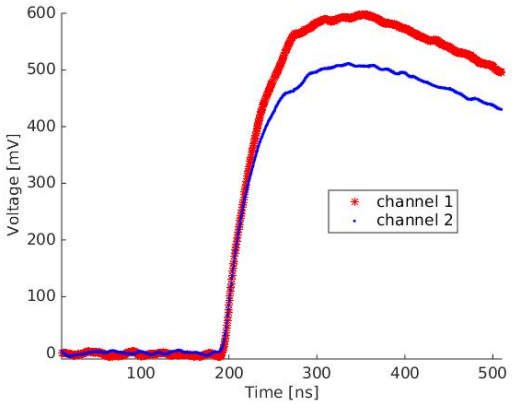
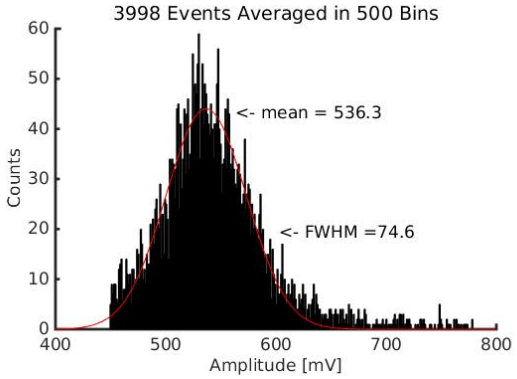


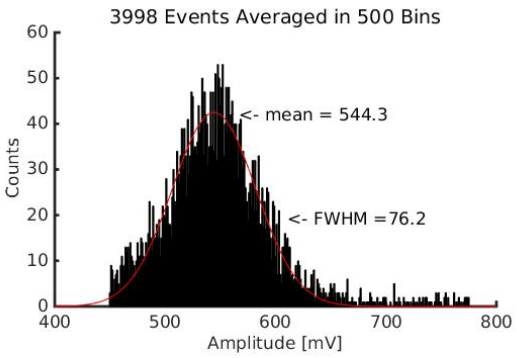
Figure 3.10: Single coincident APD event with the V3 running at 2 GSPS.

that the rise time is around 70 ns and that the waveform is not fully digitized at the given sampling speed of 2 GSPS. However, to achieve best timing performance the fastest sampling speed is chosen, where the $\frac{\Delta E}{E}$ is still acceptable. The $\frac{\Delta E}{E}$ is calculated by plotting the amplitudes of the analog signals as illustrated in fig. 3.11. The two spectra are produced with a Na-22 source. The spectra shows coincident events with energies inside the photo-peaks, only. The missing Compton continuum was discarded by the NIM electronics for this CRT-test (see fig. 2.16). The spectra bias voltages of channel #1 and channel #2 are set to 400 V.

Table 3.1 lists all other voltage results including the CRTs together with the



(a) Coincident spectrum of APD #1



(b) Coincident spectrum of APD #2

Figure 3.11: Coincident spectra of two APDs coupled to LSO with a bias voltage of 400 V.

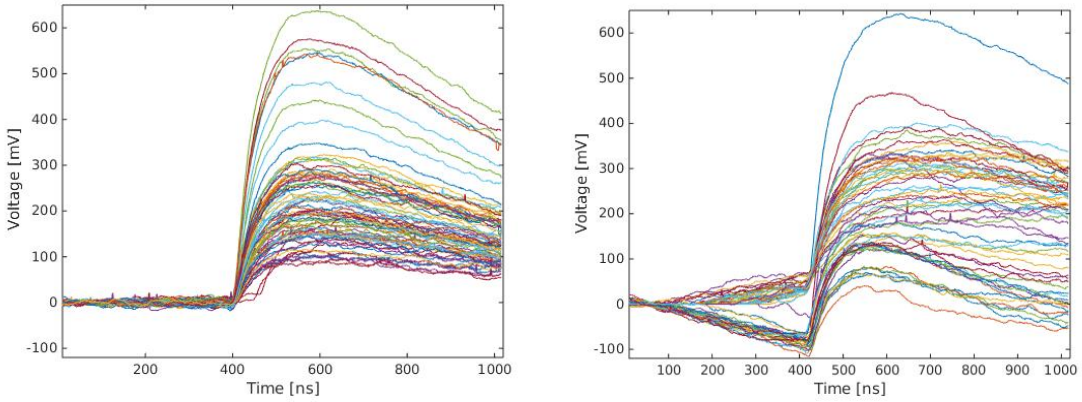
Table 3.1: CRT-test results for two APDs coupled to LSO dependent on the bias voltage.

bias voltage	$\frac{\Delta E}{E}$ channel 1	$\frac{\Delta E}{E}$ channel 2	CRT (FWHM)	TH1	TH2
360 V	14.3 % at 130 mV	14.3 % at 132 mV	1.8 ns	6%	5%
370 V	13.5 % at 182 mV	16.6 % at 185 mV	1.4 ns	5%	4%
380 V	13.3 % at 271 mV	13.5 % at 277 mV	1.3 ns	6%	4%
390 V	13.4 % at 367 mV	13.7 % at 378 mV	1.3 ns	5%	4%
400 V	13.9 % at 536 mV	14.0 % at 544 mV	1.2 ns	6%	5%
410 V	14.6 % at 832 mV	14.7 % at 851 mV	1.5 ns	6%	4%

corresponding TH values. 4000 coincident events are digitized and analyzed with a digital LED for each voltage setting. The energy information was not used to improve the CRT (no walk correction). One can see in table 3.1 that the best CRT for this CRT-test with APD lies around 1.2 ns (FWHM). This CRT is measured with a TH of 30 mV which is around 6 % of the photo-peak amplitude.

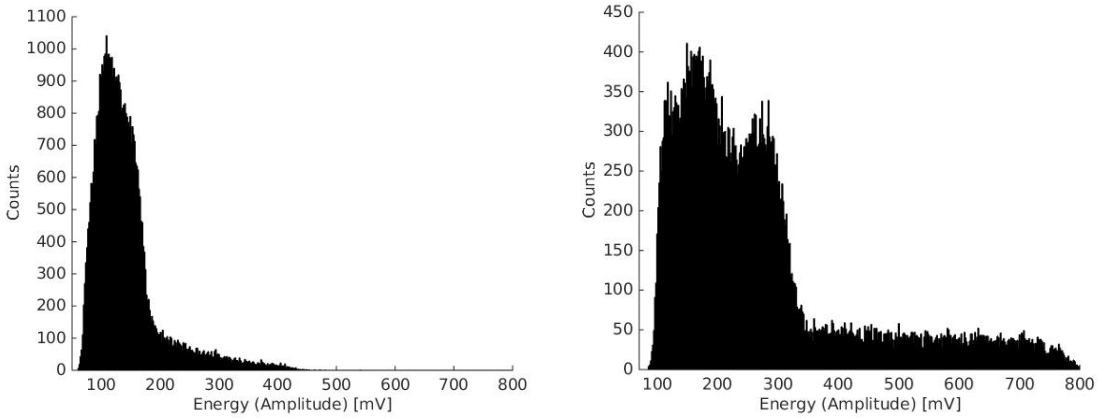
3.1.6 CRT-Test with the PET-INSERT

The same APD technology that was tested in section 3.1.5 is investigated again inside the PET-INSERT. Two facing detector-blocks inside and outside an MRI were especially investigated. More details concerning the corresponding test setup are given in section 2.5.4.

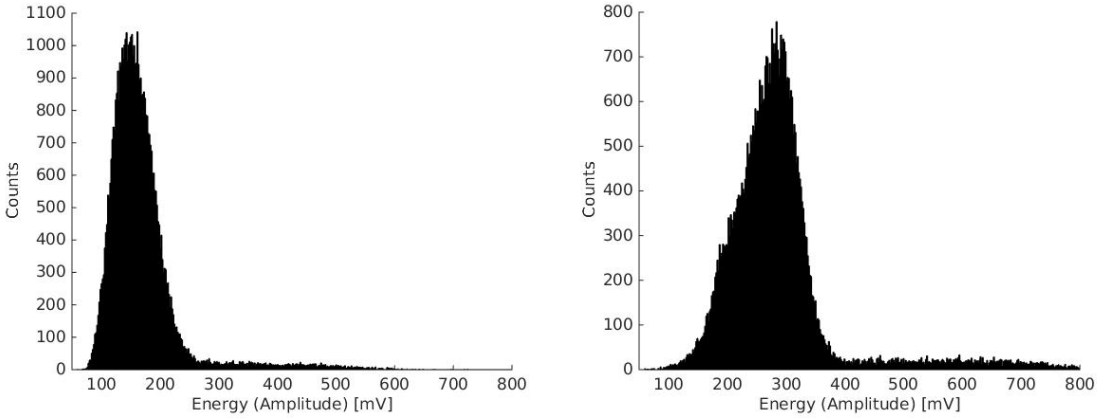


(a) outside 3 T MF **(b)** inside 3 T MF

Figure 3.12: Waveforms of block #15 (PET-INSERT) with and without MF digitized with the V3.

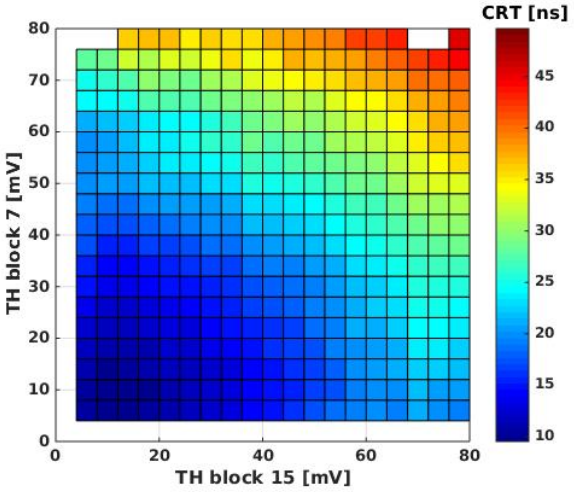


(a) energy spectrum block #7 **(b)** energy spectrum block #15

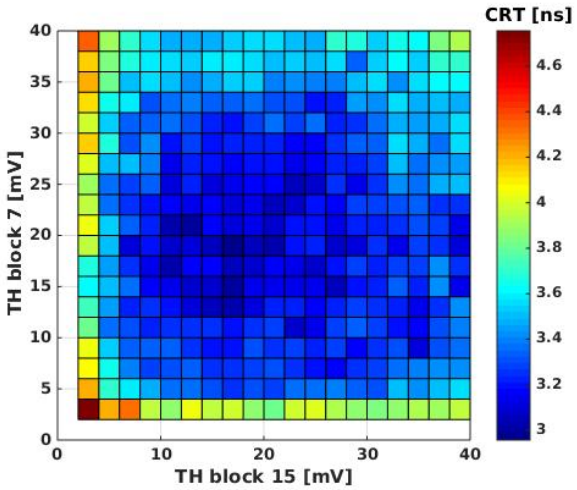


(c) energy spectrum block #7 (MF) **(d)** energy spectrum block #15 (MF)

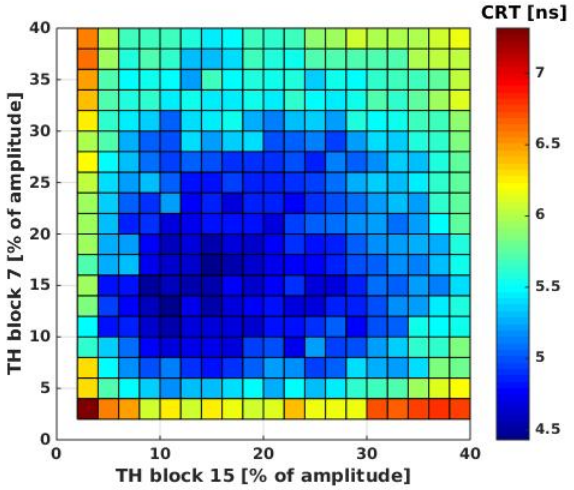
Figure 3.13: Energy spectra for the PET-INSERT utilizing the V3.



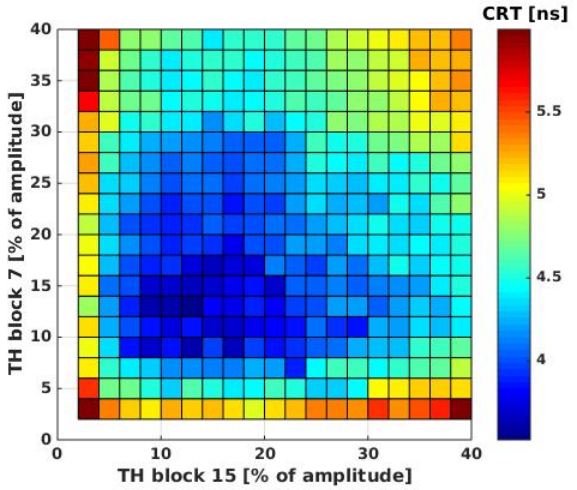
(a) walk effect, max EW, no MF (row #1)



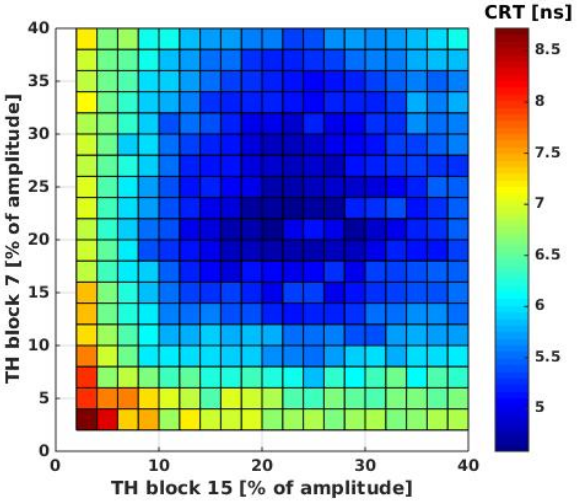
(b) walk effect, min EW, no MF (row #3)



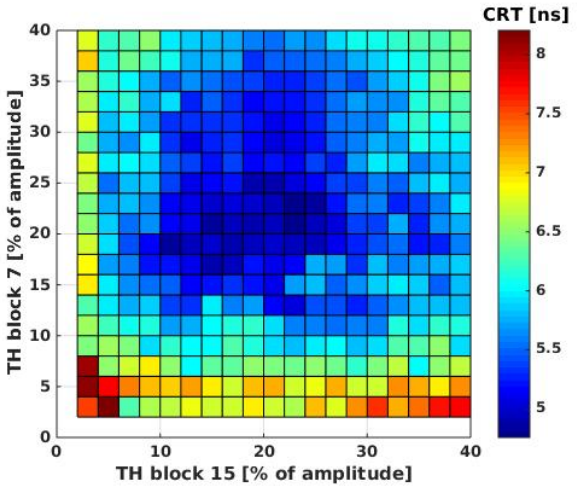
(c) lin. fit, max EW, no MF (row #4)



(d) lin. fit, narrow EW, no MF (row #5)

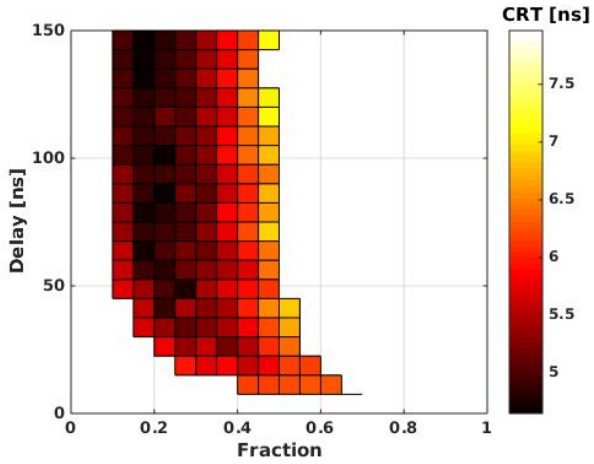


(e) spline10, max EW, MF (row #14)

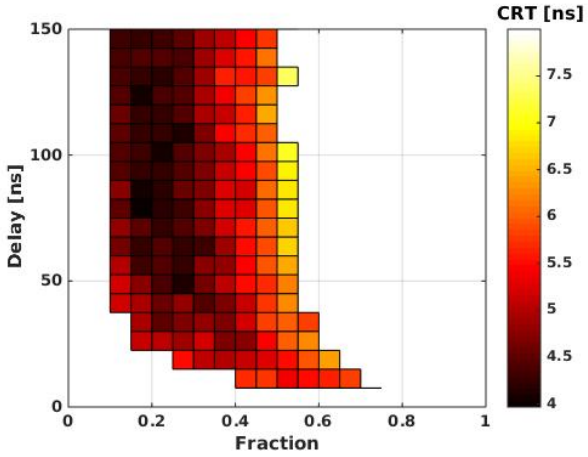


(f) spline10, narrow EW, MF (row #15)

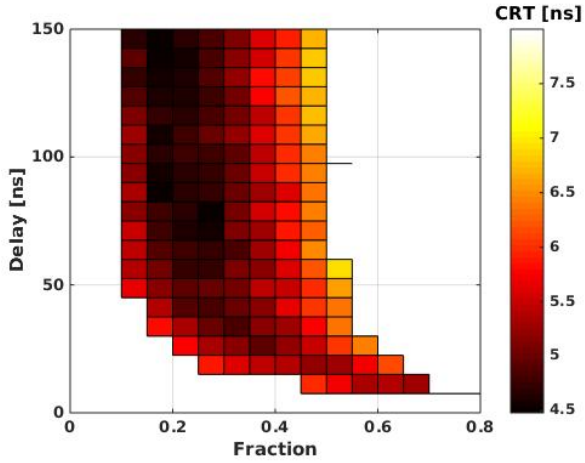
Figure 3.14: CRT-test histogram examples from table 3.2 for the PET-INSERT with different digital LED settings.



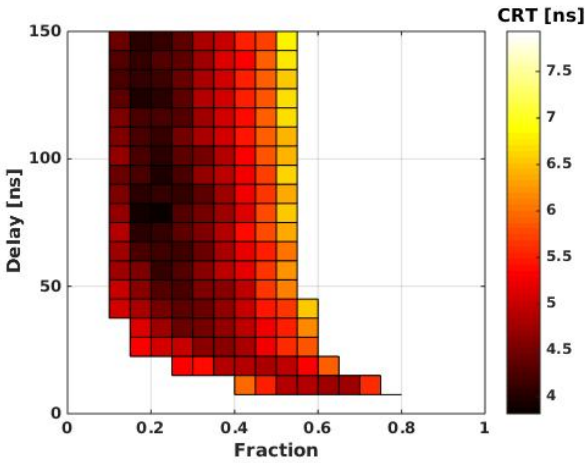
(a) lin. fit, max EW, no MF (row #1)



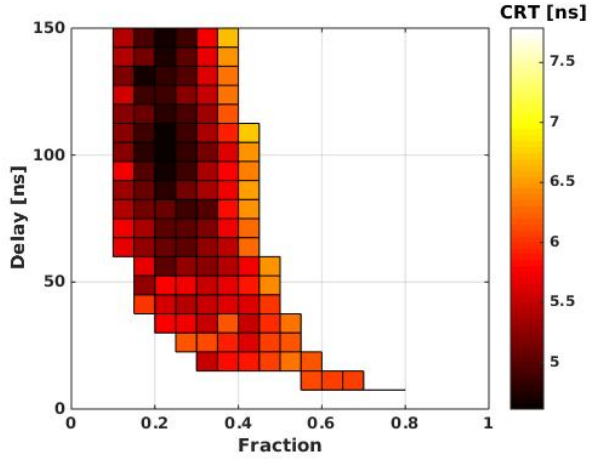
(b) lin. fit, narrow EW, no MF (row #2)



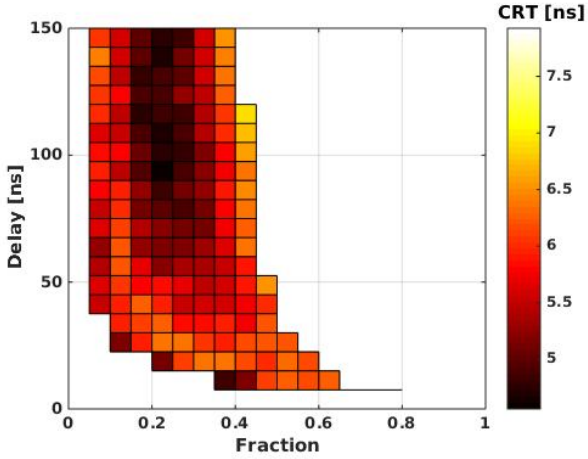
(c) spline50, max EW, no MF (row #5)



(d) spline50, narrow EW, no MF (row #6)



(e) spline10, max EW, MF (row #11)



(f) spline10, narrow EW, MF (row #12)

Figure 3.15: CRT-test histogram examples from table 3.3 for the PET-INSERT with different digital CFD settings.

Table 3.2: CRT-test results for the PET-INSERT utilizing different digital LEDs. The "#" introduces the block number.

row	method	EW #15	EW #7	TH #15	TH #7	CRT	MF	events
1	linear fit	>40 mV	>40 mV	8 mV	8 mV	9.5 ns	No	100 %
2	linear fit	>200 mV	>100 mV	32 mV	4 mV	5.9 ns	No	30 %
3	linear fit	>300 mV	>200 mV	16 mV	18 mV	2.9 ns	No	1 %
4	linear fit	>40 mV	>40 mV	10 %	12 %	4.4 ns	No	100 %
5	linear fit	>200 mV	>100 mV	12 %	12 %	3.5 ns	No	30 %
6	spline10	>40 mV	>40 mV	10 %	14 %	4.3 ns	No	100 %
7	spline10	>200 mV	>100 mV	10 %	12 %	3.5 ns	No	30 %
8	spline50	>40 mV	>40 mV	10 %	14 %	4.4 ns	No	100 %
9	spline50	>200 mV	>100 mV	14 %	12 %	3.5 ns	No	30 %
10	spline90	>40 mV	>40 mV	22 %	12 %	4.4 ns	No	100 %
11	spline90	>200 mV	>100 mV	14 %	12 %	3.6 ns	No	30 %
12	linear fit	>40 mV	>40 mV	20 %	22 %	4.7 ns	Yes	100 %
13	linear fit	>200 mV	>100 mV	20 %	20 %	4.6 ns	Yes	30 %
14	spline10	>40 mV	>40 mV	20 %	20 %	4.6 ns	Yes	100 %
15	spline10	>200 mV	>100 mV	22 %	20 %	4.8 ns	Yes	30 %
16	spline50	>40 mV	>40 mV	26 %	18 %	4.5 ns	Yes	100 %
17	spline50	>200 mV	>100 mV	16 %	20 %	4.7 ns	Yes	30 %
18	spline90	>40 mV	>40 mV	26 %	30 %	4.6 ns	Yes	100 %
19	spline90	>200 mV	>100 mV	18 %	24 %	5.0 ns	Yes	30 %

The two plots in fig. 3.12 show individual sets of a block-waveform inside and outside a 3 T *Magnetic Field* (MF). Both plots show 100 random waveforms of block #15. A single waveforms consists of the sum of all 4 channels of the block. The rise time is around 80 ns and thus this signal is slightly slower compared to the single crystal measurements with APDs in section 3.1.5. The waveforms for block #7 look identical and are therefore not shown. However, the strong impact of the gradient field on the baseline of the waveform is visible in fig. 3.12(b).

The corresponding energy distributions of the two mentioned blocks are shown in fig. 3.13. Shown are four individual block energy distributions inside and outside a 3 T MF. Each histogram consists of 800 bins (amplitude-axis) where 50000

Table 3.3: CRT-test results for the PET-INSERT utilizing different digital CFD settings. The "#" introduces the block number.

row	method	EW #15	EW #7	fraction	delay	CRT	MF	events
1	linear fit	>40 mV	>40 mV	15 %	135 ns	4.7 ns	No	100 %
2	linear fit	>200 mV	>100 mV	15 %	75 ns	4.0 ns	No	30 %
3	spline10	>40 mV	>40 mV	15 %	83 ns	4.5 ns	No	100 %
4	spline10	>200 mV	>100 mV	20 %	75 ns	4.0 ns	No	30 %
5	spline50	>40 mV	>40 mV	15 %	135 ns	4.5 ns	No	100 %
6	spline50	>200 mV	>100 mV	20 %	75 ns	3.8 ns	No	30 %
7	spline90	>40 mV	>40 mV	20 %	143 ns	4.6 ns	No	100 %
8	spline90	>200 mV	>100 mV	20 %	83 ns	3.9 ns	No	30 %
9	linear fit	>40 mV	>40 mV	15 %	113 ns	4.7 ns	Yes	100 %
10	linear fit	>200 mV	>100 mV	15 %	113 ns	4.8 ns	Yes	30 %
11	spline10	>40 mV	>40 mV	20 %	135 ns	4.6 ns	Yes	100 %
12	spline10	>200 mV	>100 mV	15 %	98 ns	4.7 ns	Yes	30 %
13	spline50	>40 mV	>40 mV	20 %	105 ns	4.6 ns	Yes	100 %
14	spline50	>200 mV	>100 mV	20 %	90 ns	4.6 ns	Yes	30 %
15	spline90	>40 mV	>40 mV	20 %	93 ns	4.8 ns	Yes	100 %
16	spline90	>200 mV	>100 mV	20 %	20 ns	4.8 ns	Yes	30 %

waveforms are analyzed for $\frac{\Delta E}{E}$. The energy distributions originate from coincident events between block #7 and block #15 within a 40 ns time window. The energy of a PET-event is calculated as amplitude and not as the integral over the curve. Each amplitude is computed individually for all waveforms by subtracting the highest point from the lowest point. To be specific, the average of 10 surrounding points of the highest point and the average of 10 surrounding points of the lowest point have been used for the subtraction. The integral of the waveform is usually used to calculate the energy. However, in this special case where the baseline shows such a noisy behavior the prior mentioned method works better. One can see in fig. 3.13(a & b) that the amplitude of the 511 keV photo-peak is around 300 mV for the block #15 and 150 mV for block #7. The influence of the 3 T MF is clearly visible for the $\frac{\Delta E}{E}$ in fig. 3.13(c & d).

A digital LED and a digital CFD are used for this CRT-test. The energy infor-

mation is used in some cases to correct for the walk effect when a digital LED is utilized. Additionally, an *Energy Window* (EW) is uses to reject Compton scattered events. A 2-points linear fit interpolation (lin. fit) and a spline fit interpolation is utilized for both discriminators to compute the time information. The smoothing factor for the spline fit is set to 10 % (spline10), 50 % (spline50) and 90 % (spline90).

Table 3.2 summarizes the best CRT results for the PET-INSERT when varying the digital LED settings. The illustrated settings in table 3.2 are the 2-points linear fit, different spline fits, a walk correction (symbolized by the TH measured in " %"), the MF measurements and an EW selection. For example row #2 in table 3.2 shows a comparable poor CRT outcome of 5.9 ns (FWHM) which is a result of the walk effect although 70% of the low-energy events have been rejected. Additionally, six selected examples from table 3.2 are available in more detail in fig. 3.14, where the CRT dependent on both TH values are displayed. For example fig. 3.14(a) corresponds to row #1 of table 3.2 as reproducible with the labeling "lin. fit, walk effect, EW: >40 mV, no MF".

Table 3.3 shows the results of all digital CFD settings. One will find similar settings with a slight modification as in the previously mentioned table 3.2. Both TH settings are replaced with two CFD parameters, which are the fraction and the delay. Consequently, six chosen examples from table 3.3 are displayed again as 2D-matrices in fig. 3.15. The 2D-matrices show the CRT dependent on delay and fraction. The white regions within the 2D-matrices stand for combinations of the delay vs. the fraction that are excluded. The digital CFD algorithm starts to loose events in these regions.

3.2 X742 when Utilizing its Dedicated Calibrations

Both versions of the X742 are tested in this section together with their original calibrations provided by CAEN. General test results (e.g. data transmission speed) are first provided as in the previous section 3.1. Afterwards the baseline noise is investigated. Finally, the time resolution is evaluated in the following 3 sub-sections.

The DT5742 can transmit with the fastest PC around 2000 acquisitions/s, when

all calibrations are turned off. When both DRS4-chips are used, the data rate decreases by half. A realistic scenario is 600-800 acquisitions/s when utilizing all 16 channels.

The V1742 is less sensitive to the PC used. Its data rate is around 6000 acquisitions/s with all calibrations turned off. A realistic scenario is around 1000 acquisitions/s when utilizing all 32 channels. The acquisition rates of the X742 can be increased by accessing only one DRS4-chip . Alternatively, one can increase the acquisition rate if not all 1024 SPs of a channel are digitized. The four options are 1024, 520, 256 and 136 SPs.

The dynamic range of the X742 chosen by CAEN is identical to the V3 as 1 V peak-to-peak, but with the advantage that the DC-level of each channel is individually adjustable. The digitized SPs are provided in ADC values from 0 to 4095 corresponding to a dynamic range of 1 V peak-to-peak.

Illustrated in fig. 3.16 is the dynamic range test of channel #18, where a 100 MHz sine wave is digitized with a sampling speed of 5 GSPS. The peak-to-peak value of

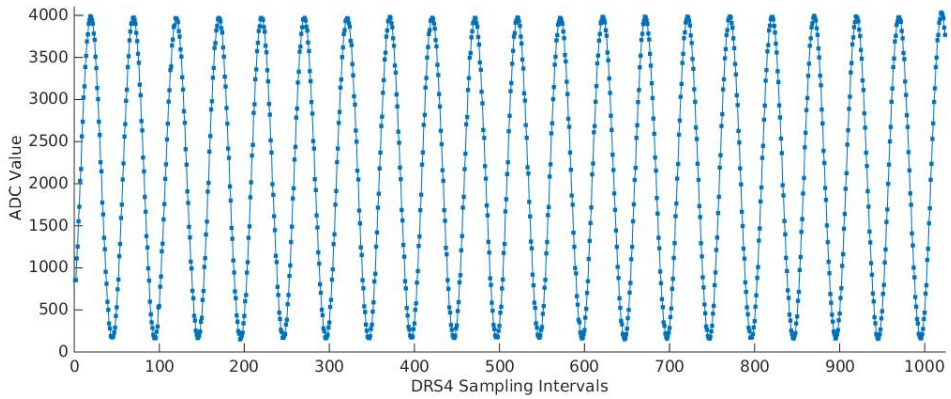
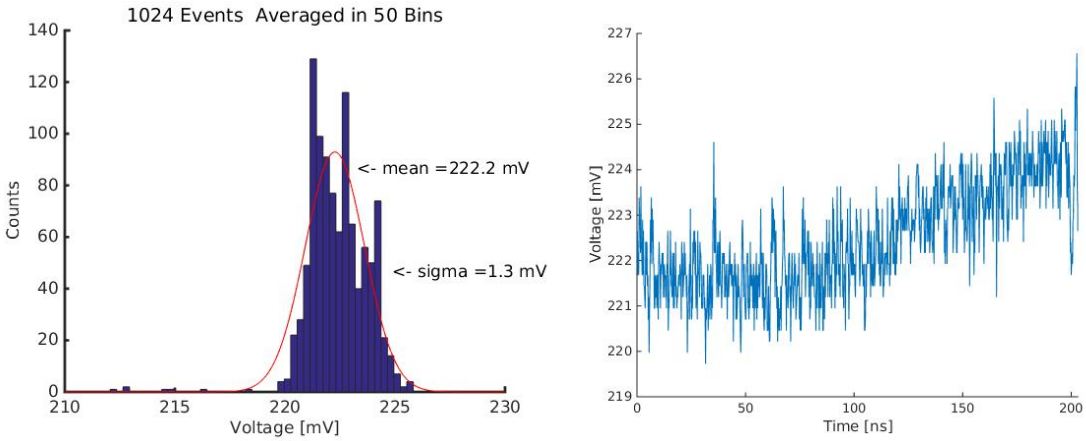


Figure 3.16: 100 MHz sine wave digitized at 5 GHz with the V1742.

the sine wave is 1 V, which corresponds to an ADC output of around 3850 (peak-to-peak). The other channels of this board result in similar outcomes. Thus, the dynamic range of this V1742 is around 1.064 V (peak-to-peak).

That the baseline noise of the V1742 varies dependent on the trigger rate is investigated. Its smallest value results from low trigger rates (for example 100 Hz), selecting all four DRS4-chips and digitizing all 1024 SPs. The worst case scenario is displayed in two formats in fig. 3.17. First, a histogram is shown illustrating a



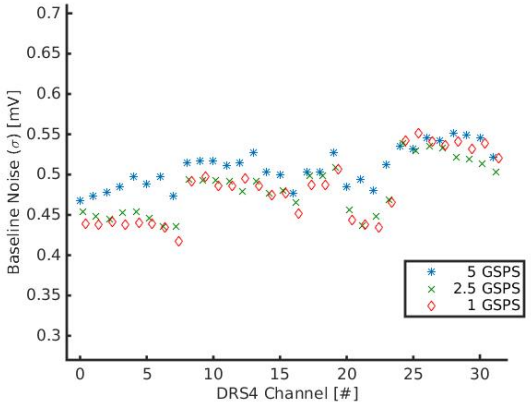
(a) Noise spectrum of all cells **(b)** Single baseline waveform

Figure 3.17: Typical baseline noise of the V1742 at 5 GSPS when triggering with 10 kHz.

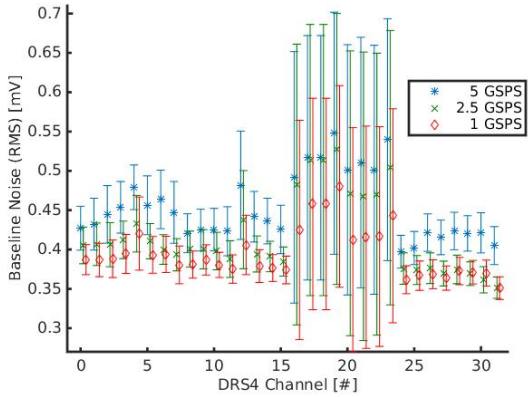
DC-offset of around 220 mV which resulted from a single waveform in fig. 3.17(a). One can also see a relatively high baseline fluctuation of the 1024 SPs. Second, in fig. 3.17(b) only the first 1020 SPs of the same waveform are plotted over time. The last 4 SPs are outliers and therefore rejected. For this measurement an input trigger rate of 10 kHz results in around 4000 acquisition/s. In addition, only one DRS4-chip is selected and running at 5 GSPS (V1742).

Fig. 3.18 shows the baseline noise behavior when triggering at 66 Hz (all DRS4-chips activated) and utilizing four different analyzing methods. In all four cases channel #18 is a copy of channel #17. The 100 MHz sine wave which is illustrated in fig. 3.16 is applied to channel #18 for testing the cross-talk between neighboring channels. All plots (a-d) illustrate the baseline noise of the same dataset of 1000 waveforms dependent on the V1742-channel when utilizing different analyzing techniques. Fig. 3.18(a) shows the baseline noise when histogramming (Gaussian fit) all SPs of all 1000 waveforms at once. In fig. 3.18(c & d) the histogramming is performed waveform by waveform. For fig. 3.18(d) only the first 500 SPs of the 1024 SPs are utilized and for fig. 3.18(b) the RMS values are used instead of a Gaussian fit.

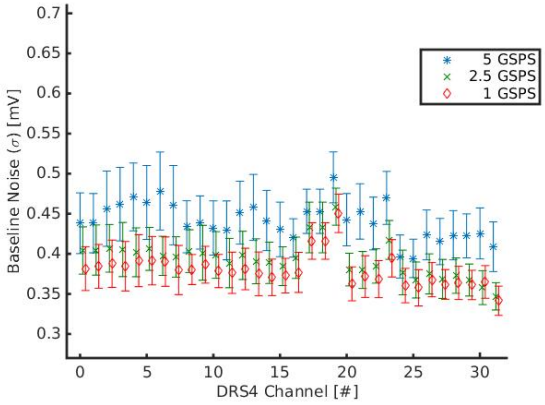
The spike probability is summarized in table 3.4 for various scenarios. It shows that it is dependent on the available c_{stop} positions, the f_{SCA} and the individual DRS4-chip. It should also be mentioned that the same cells will always show the



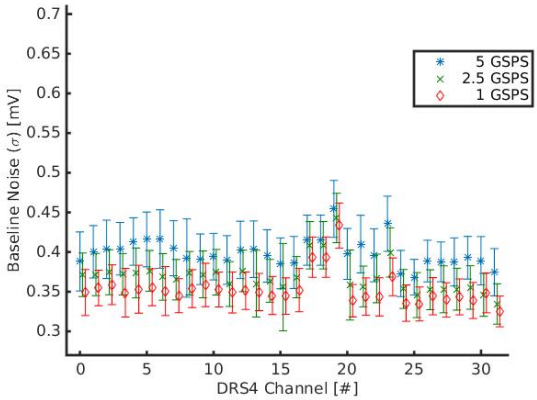
(a) σ noise of 32×1024000 SPs



(b) RMS noise of $32 \times 1024 \times 1000$ SPs



(c) σ noise of $32 \times 1024 \times 1000$ SPs



(d) σ noise of $32 \times 500 \times 1000$ SPs

Figure 3.18: Illustrated is the baselines noise of 1000 baseline measurements for all 32 channels and three f_{SCA}. The V1742 is triggered at a rate of 66 Hz.

spike behavior with a certain probability, which is different from the V3. When looking at table 3.4 row #1, the overall probability to measure a symmetrical spike event is 31 %. One can also see that three scenarios can happen at 5 GSPS in row #1. What's not visible in row #1 is that two of these scenarios appear with a probability of roughly 15 % and one with a probability smaller than 1 %. In fig. 3.19(c) the spike scenarios are visualized for a 1 GSPS case[I]. However, in all scenarios the spikes will occur at the same cell position[II]. Additionally, the spike position shift

[I] Table 3.4 predicts 15 scenarios for this sampling speed. However, one can only see 12 of the 15 expected scenarios in fig. 3.19(c). 23 (22 symmetrical) double-spikes are visible and one is hidden at zero in the y-axis. The probability for the missing three scenarios occurring is much smaller than 1% and therefore not visible in this example.

[II] In some cases (much smaller than 1%) the position is fluctuating one cell position away from the predictable cell position.

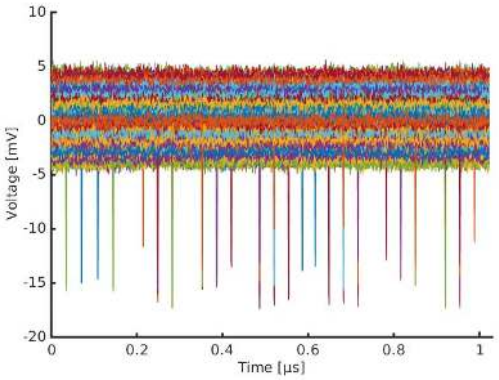
Table 3.4: Summary of the measured spikes behavior when utilizing the V1742 at all sampling speeds.

DRS4-chip #	c_{stop} positions	f_{SCA}	probability	scenarios	distance
group # 0	24 (fast trig.)	5 GSPS	31 %	3	∼172 samples
group # 0	48 (fast trig.)	2.5 GSPS	35 %	6	∼85 samples
group # 0	120 (fast trig.)	1 GSPS	28 %	15	∼34 samples
group # 2	6 (glob. trig.)	5 GSPS	16 %	3	∼172 samples
group # 2	12 (glob. trig.)	2.5 GSPS	20 %	6	∼85 samples
group # 2	30 (glob. trig.)	1 GSPS	9 %	15	∼34 samples

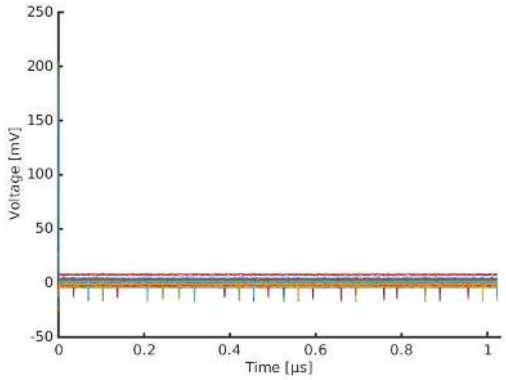
between scenarios appears with a predictable pattern (distance) as illustrated in table 3.4. For better understanding all three measured 4-spike events of row #1, the naming of cell positions will be provided as (12,13,1010,1011), (182,183,840,841) and (356,357,666,667). The first cell position always defines the following 3 cell positions. Thus, one can simplify the three scenarios as cell position 12, 182 and 356. With this simplified writing, one can see that scenarios are predictable with multiples of around 172 samples (around 33 ns) from a previous measured spike scenario.

The spike positions did not change by varying the trigger rate. Fig. 3.19 illustrates that the c_{stop} also has no dependency on the spike positions. The positions are individual for every DRS4-chip at a given sampling speed. It should be mentioned that the noise of the first SP is dramatically increased when stopped at one of the spike candidates as illustrated in fig. 3.19(b & d). The spike probability did not change for the two tested c_{stop}. Both c_{stop} are randomly triggered 500 times. Exactly 428 spikes (107 symmetrical double-spike events) are measured for c_{stop}=249. For c_{stop}=603 a similar amount (99 symmetrical double-spike events) occur when subtracting the 445 wrong spikes (caused by c_{stop}=603) from the 841 measured spikes.

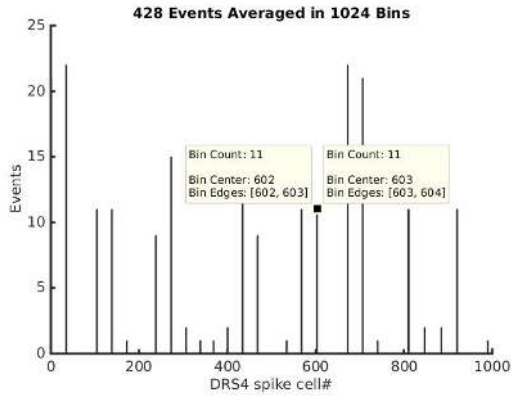
The X742 sampling can be stopped either by a fast trigger channel or a global trigger channel. However, the DRS4-chip cannot be stopped at every c_{stop}. As illustrated in table 3.4 the global trigger channel allows only 6 equidistant c_{stop} positions (around 33 ns steps) simultaneously for all DRS4-chips when sampling at



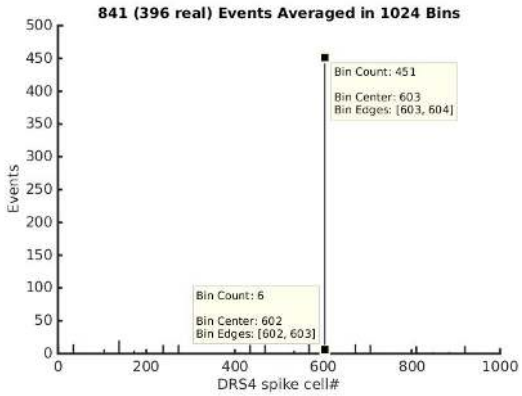
(a) 500 waveforms at c_{stop}=249



(b) 500 waveforms at c_{stop}=603



(c) 107 spike-pair events (c_{stop}=249)



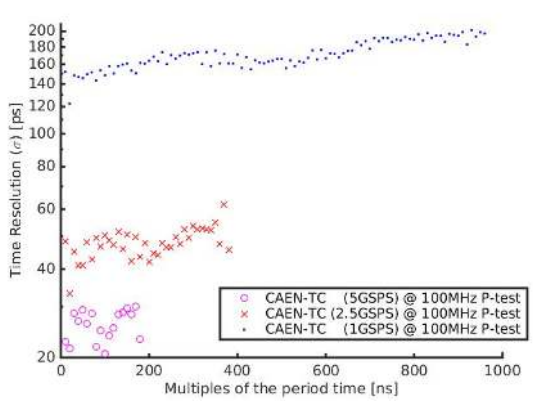
(d) 99 spike-pair events (c_{stop}=603)

Figure 3.19: Illustrated in (a) and (b)are the baselines of 500 baseline measurements from channel #1 (V1742) sampling at 1 GSPS when stopped at two individual c_{stop} positions. (c) and (d) show the dedicated spike counts and positions.

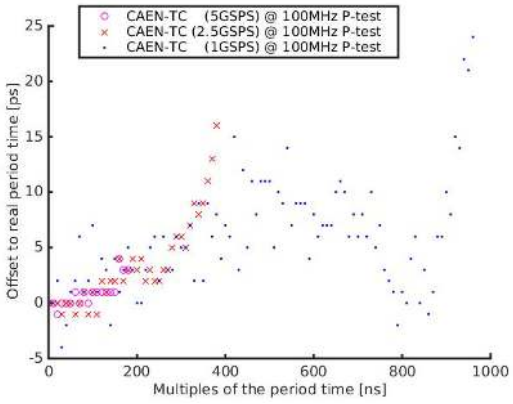
5 GSPS. Fewer c_{stop} positions makes it easier for CAEN to synchronize all DRS4-chips. Synchronizing improves the time resolution according to former measurements from PSI. Therefore, the waveform positions in all channels will fluctuate more than 30 ns if a measurement is repeated with the global trigger. Also it can trigger up to four DRS4-chips simultaneously. The response time to stop a DRS4-chip after the global trigger was measured to be around 260 ns.

In contrast, the fast channel can trigger up to two DRS4-chips simultaneously. However, the absolute number of allowed c_{stop} is four times higher compared to the global trigger channel. Additionally, the fast trigger channel is digitized in the ninth channel of each DRS4-chip. Finally, the faster response time should be mentioned which is approximately 30 ns and thus similar to the V3.

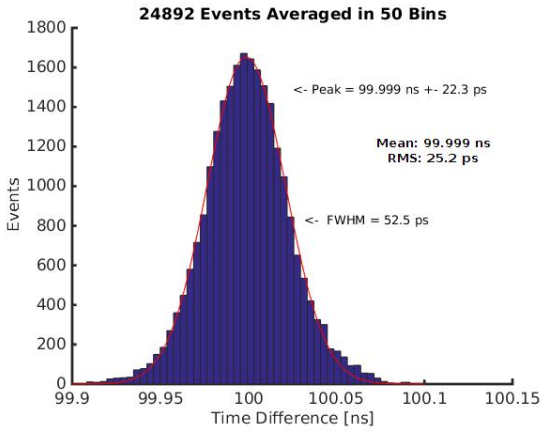
3.2.1 P-Test



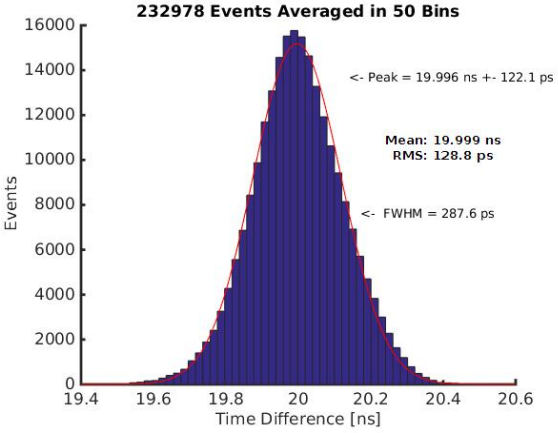
(a) σ values of P-test



(b) Offset of P-test



(c) 5 GSPS example expecting 100 ns



(d) 1 GSPS example expecting 20 ns

Figure 3.20: The P-test in (a) shows the time resolution (σ) vs. the delay (100 MHz) for the V1742 (CAEN-TC) and (b) illustrates its corresponding offset vs. the delay. (c) and (d) illustrate two individual time resolution histograms from (a).

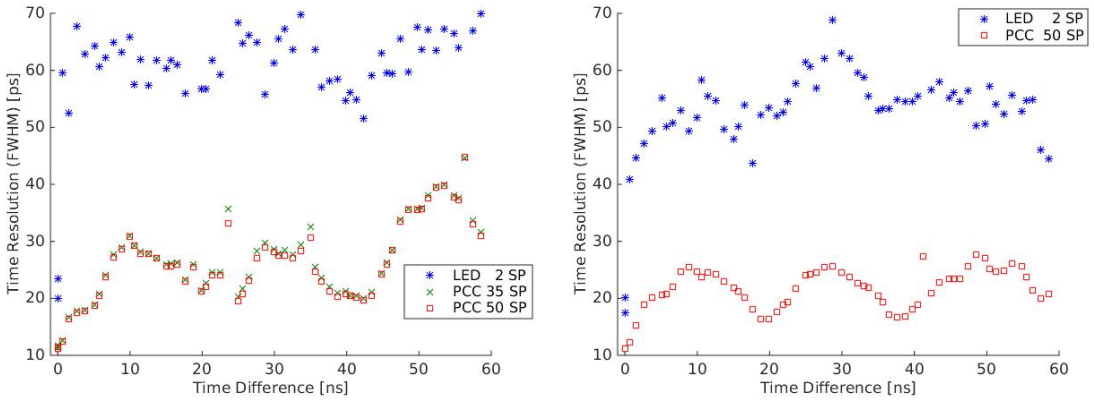
In this sub-section the P-test for all three sampling speeds (5 GSPS, 2.5 GSPS and 1 GSPS) of the V1742 can be found in fig. 3.20, when applying its default settings (CAEN-VC & CAEN-TC). One can see in fig. 3.20(a) that the standard deviation is around 25 ps for 5 GSPS, around 50 ps for 2.5 GSPS and around 160 ps for 1 GSPS. All three sampling speeds show a time resolution inconsistency depending on the delay. The offset in fig. 3.20(b) shows the maximum error from the true delay which is around 5 ps for 5 GSPS, around 16 ps for 2.5 GSPS and less than 25 ps for 1 GSPS. Two histogram examples of the multiples of the 100 MHz sine wave are additionally

given in fig. 3.20. One can see that all histograms show a Gaussian like distribution. This is why the RMS values and σ in fig. 3.20(c & d) are similar. Thus, also the mean value and the fitted peak show a similar outcome. An example can be found in fig. 3.20(d). All other distributions which are not illustrated show similar behavior.

3.2.2 SP-Test

The SP-test is applied to the V1742 when running at 5 GSPS in this sub-section. 10k events are collected for each cable delay. As an exception, all time resolution results are given in FWHM for this SP-test. Using FWHM instead of σ is convenient for predicting the effect of this readout electronics on PET measurements which is also measured in FWHM. More details about the SP-test are available in section 2.5.2.

Two SP-test results are shown in fig. 3.21. Both plots (a & b) show the time resolution (FWHM) vs. the time differences of the cable delay. A digital LED and



(a) SP-test between channel#16 and #17 **(b)** SP-test between channel#24 and #25

Figure 3.21: SP-test (digital LED and PCC) for the V1742 (CAEN-TC) when running at 5 GSPS.

the PCC are visualized in both plots for two neighboring channels of individual DRS4-chips. The digital LED calculates the time at the given TH of 300 mV by using only 2 SPs. One can see that all time resolutions of both digital LEDs rapidly increase up to a delay of around 3 ns and later vary between 45 ps and 70 ps (FWHM).

The first SP is 10 SPs left of the given TH for the PCC and four templates have been produced, one for each channel. Each template is computed out of 1 million

events. In (a) two different cases for the PCC are investigated using 35 SPs and 50 SPs. The PCC shows no major differences if 35 SPs or 50 SPs are used. However, all PCCs clearly improve the time resolution compared to the results of the digital LED. The improved time resolution oscillates between 10 ps and 30 ps (FWHM). All three PCC curves indicate a sine wave which is similar to the V3 results in section 3.1.2. This time 50 MHz can be approximated.

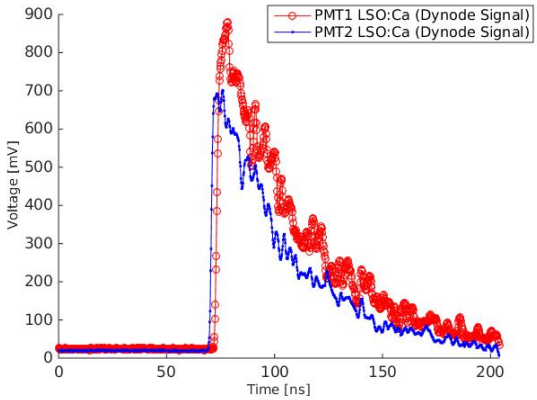
3.2.3 CRT-Test with PMTs Coupled to LSO:Ca

The CRT-test results of two fast PMTs coupled to LSO:Ca-crystals are found in this sub-section. The DT5742 (CAEN-TC) is utilized as readout electronics when running at 5 GSPS. Only the dynode outputs have been analyzed. 100k coincident events have been collected individually for both delay scenarios. More information about the experiment can be found in section 2.5 and particularly in section 2.5.6.

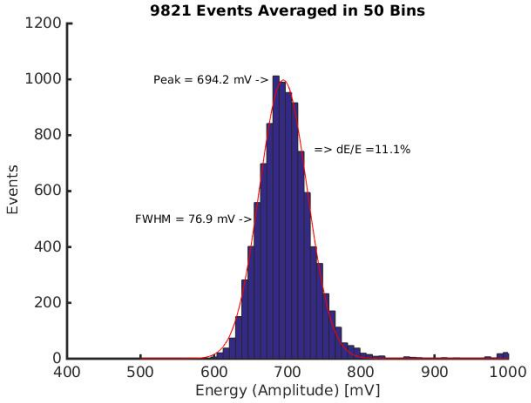
Fig. 3.22(a) shows the digitized coincident waveforms of channel #1 and channel #2 . One can see that the rise time is around 2 ns. Fig. 3.22(b & c) illustrate the $\frac{\Delta E}{E}$ of both channels when only the amplitudes are measured. In this case the $\frac{\Delta E}{E}$ is around 11% for channel #1 and 13% for channel #2. Further in fig. 3.22(d & e) the $\frac{\Delta E}{E}$ is shown when the integrals under the individual waveforms are calculated. The $\frac{\Delta E}{E}$ improves to around 8% for channel #1 and 9% for channel #2 with this method.

The CRT-test results for two scenarios are shown in fig. 3.23. Both input signals arrive exactly at the same time (almost 0 cm delay) in the first scenario. A digital LED is utilized with walk correction for this CRT-test. The walk correction is achieved by normalizing the waveform with the averaged photo-peak. Therefore, all TH settings for the first scenario use the unit " % ". In the second scenario the cable delay has been changed between both PMT channels to a delay of around 50 cm. For this CRT-test a digital LED (no walk correction) is utilized and thus all TH setting use the unit " mV ".

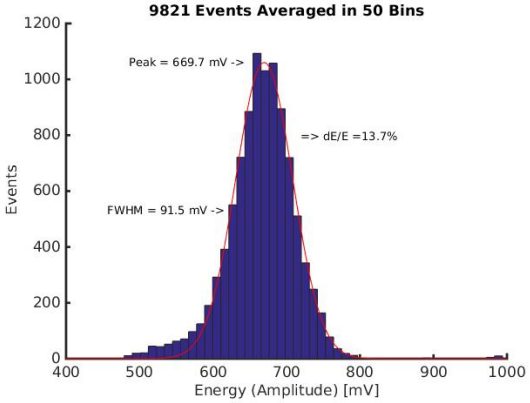
The time resolution (FWHM) vs. THs of the CRT-test is shown in form of a 2D-matrix in fig. 3.23(a & b). The dedicated measured delays of (a & b) are found in fig. 3.23(c & d). Both 2D-matrices (a & b) show unexpected patterns which correlate to the measured delay pattern in (c & d). The dedicated best timing histograms



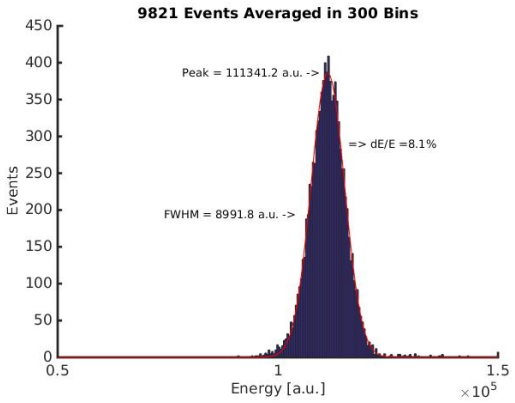
(a) Digitized coincident event with 50 cm delay



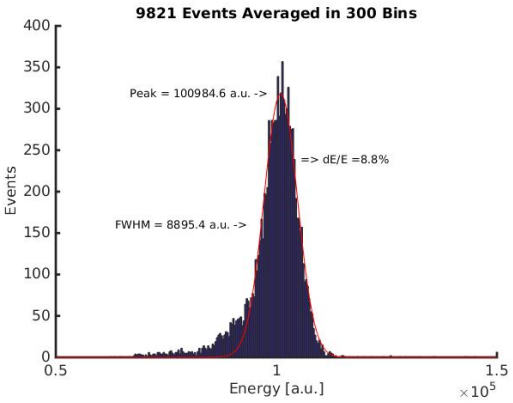
(b) Amplitude distribution for channel #1



(c) Amplitude distribution for channel #2

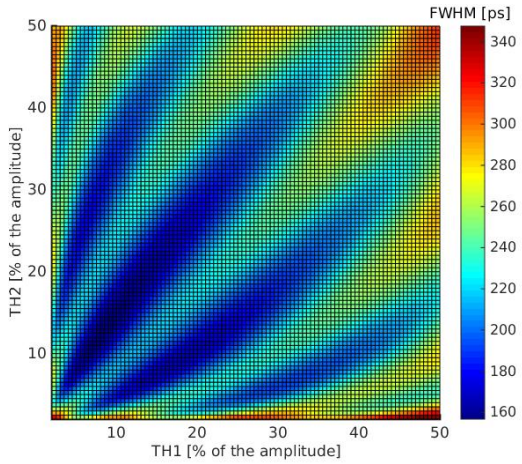


(d) Energy distribution for channel #1

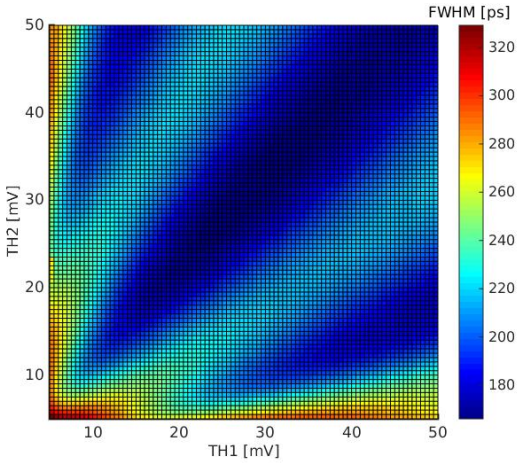


(e) Energy distribution for channel #2

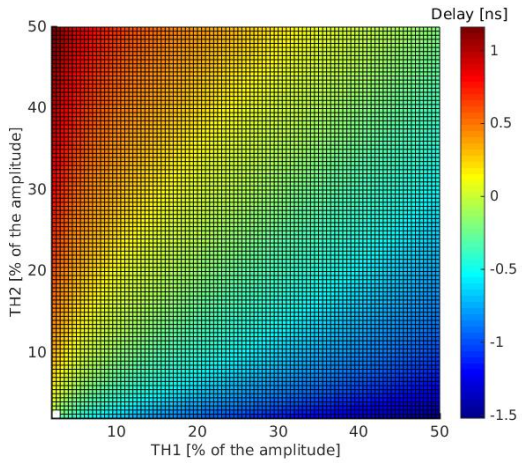
Figure 3.22: Waveform example and $\frac{\Delta E}{E}$ of two fast PMTs coupled to LSO:Ca and digitized with the X742 (CAEN-TC) at 5 GSPS.



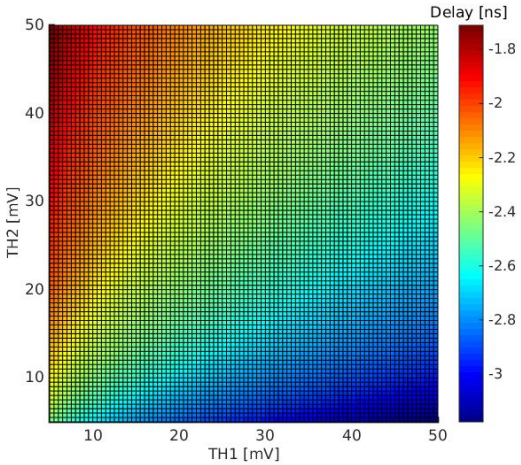
(a) CRT-test at 0 cm delay



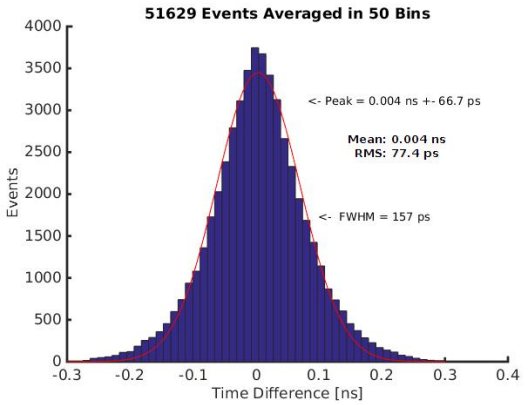
(b) CRT-test at 50 cm delay



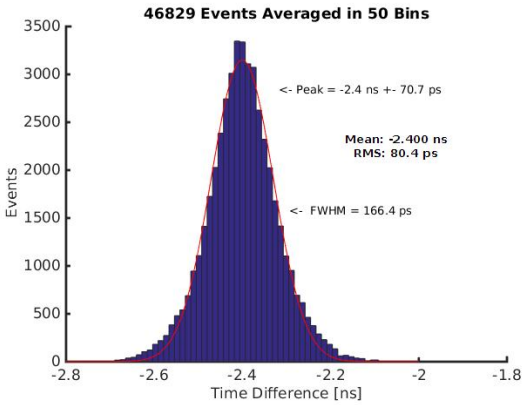
(c) Measured delay at 0 cm delay



(d) Measured delay at 50 cm delay



(e) Best timing histogram at 0 cm delay



(f) Best timing histogram at 50 cm delay

Figure 3.23: CRT-test with two fast PMTs coupled to LSO:Ca for a CAEN-calibrated DRS4 running at 5 GSPS.

of (a & b) are illustrated in fig. 3.23(e & f) and show non-Gaussian distributions. However, the best timing resolution for the 50 cm delay is 166 ps (FWHM) with TH settings of 28 mV (TH1) and 31 mV (TH2). A slightly improved timing resolution for the 0 cm delay results in 157 ps (FWHM) with TH settings around 8 % (TH1) and 12.5 % (TH2).

This experiment is repeated with an ideal TC (see section 3.4.1) and a fast readout electronics (see section 3.5.3).

3.3 V3 when Utilizing new Calibrations

The V3 results of the new developed SCA techniques[III] are found in this section. Also included is the temperature dependency of the DRS4. A minimum warm-up time of 30 minutes with an environmental temperature of 20 °C can be assumed for all results unless otherwise specified.

The impact of the environmental temperature on the V3 performance is investigated in a temperature chamber. Table 3.5 summarizes the tested V3 temperatures measured with its internal sensor (inside) vs. the environmental temperature (outside). Each of these experiments started one hour after both temperatures were

Table 3.5: Listed are both the environmental temperature outside the V3 and its corresponding temperature inside the V3 provided by the V3-board.

outside (°C)	5.1	10.0	15.1	20.0	25.0	30.0	35.0	40.0
inside (°C)	18.4	23.4	28.3	32.8	36.9	40.8	45.4	50.1
ΔT (°C)	13.3	13.4	13.2	12.8	11.9	10.8	10.4	10.1

constant. The V3 aluminum case was not used. At room temperature the V3 increased to 45 °C after 30 minutes and stabilized to 47 °C after one hour. Thus, under realistic conditions (aluminum case & 20 °C), the V3 temperature is around 15 °C higher compared to table 3.5.

[III] Details about the NEW-TCs are available in section 2.2 and further information about the NEW-VC in section 2.3.8.

The NEW-VC technique showed no measurable improvement versus the V3-VC when comparing both resulting baselines. The results are listed in table 3.13. A comparison between the most relevant NEW-TCs is available in the following sub-section 3.3.1.

3.3.1 P-Test for Comparison of all TC-Methods at 5GSPS

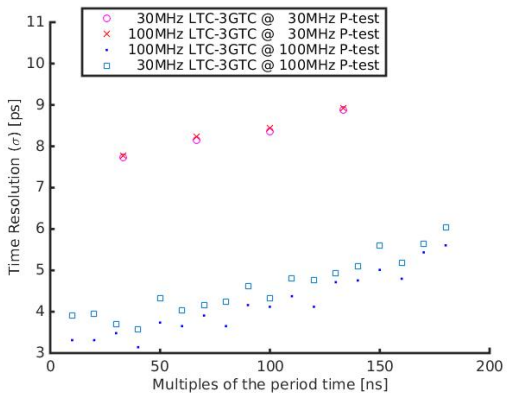
The most relevant NEW-TCs[IV] are tested in this sub-section. For the following tests the V3 is preset to 5.12 GSPS. The V3 results, unless otherwise specified, are shown for the left state[V] which means that channel #1 is always occupied and guarantees the two-state-effect identification. The NEW-TCs are tested by utilizing the P-test. The P-test is usually performed with a test frequency of 100 MHz which is equivalent to the labeling "100 MHz P-test". The LTC+3GTC is chosen to be the reference method of the NEW-TCs for the following P-tests.

Fig. 3.24 shows three typical performance examples (P-tests) for the LTC+3GTC. All plots on the left show the time resolution (σ) vs. the delay while the other side shows their corresponding offsets. Fig. 3.24(a & b) illustrates the P-test results between 30 MHz and 100 MHz sine waves of which four combinations are shown for the f_{TC} and the test frequency (see legend). One can see that the time resolution degrades when a test frequency of 30 MHz is used for the P-test. This also explains why f_{TC}=100 MHz performs better compared to f_{TC}=30 MHz. The results of the self calibration of the V3 with its internal 66 MHz clock are further demonstrated in fig. 3.24(c & d). The offset result shows that the provided f_{TC} information of 66 MHz is wrong. Fig. 3.24(d) shows that the P-test offset is around 6 ps faster for a T_{SCA} of 200 ns and thus the true f_{TC} lies around 66.002 MHz[VI]. The P-test of the 66.002 MHz clock compared to the 100 MHz sine wave shows a better time resolution because of the fast clock edges. One can see the channel dependency of the DRS4 investigated with the 100 MHz P-test at the bottom of fig. 3.24(e & f). The NEW-TC of channel #2 (ch2) and of channel #4 (ch4) is applied to individual

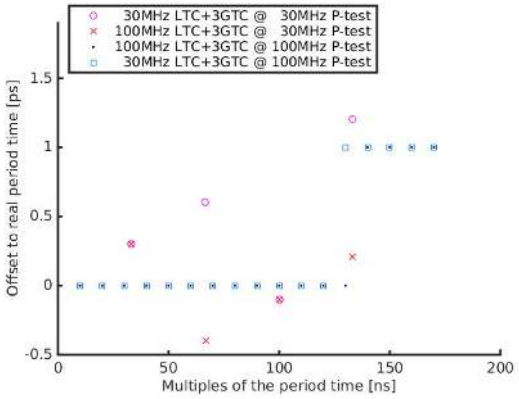
[IV] A detailed introduction to the most relevant NEW-TCs is available in section 2.2.7.

[V] More details of the two-state-effect can be found in section 3.1.

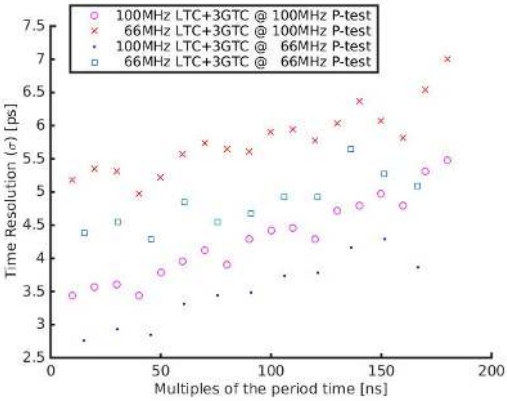
[VI] A single 66 MHz period ($15.\overline{15}$ ns) fits around 13 times in 200 ns. Thus, the true period is approximately 0.5 ps shorter and results roughly in 66.002 MHz.



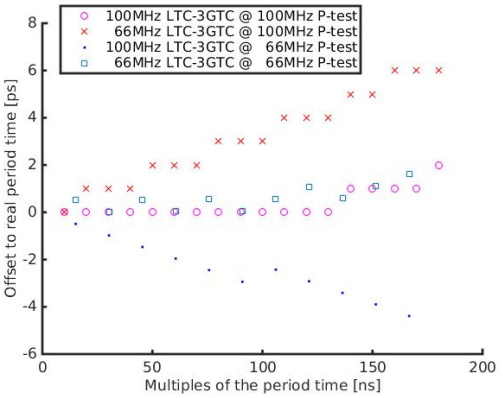
(a) σ values of P-test (30 MHz vs. 100 MHz)



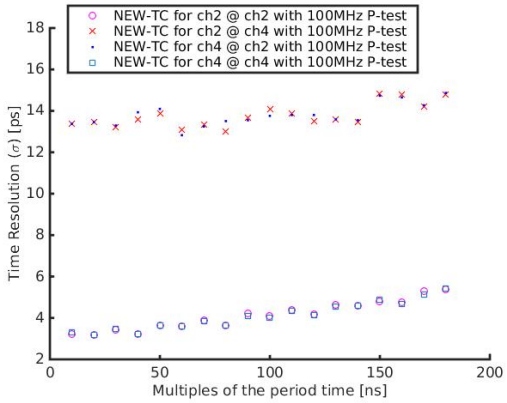
(b) Offset of P-test (30 MHz vs. 100 MHz)



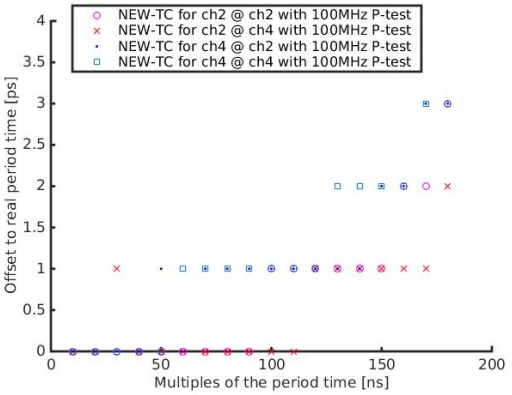
(c) σ values of P-test (internal 66 MHz clock)



(d) Offset of P-test (internal 66 MHz clock)



(e) σ values of P-test (ch2 vs. ch4)



(f) Offset of P-test (ch2 vs. ch4)

Figure 3.24: Three P-test scenarios when utilizing the NEW-TC. In each, four combinations are shown (see legend). The plots on the left show the σ values. Their dedicated offsets can be found on the right. V3 is preset to 5.12 GSPS.

channels of the V3. A performance loss of around 13 ps (σ) becomes visible if the NEW-TC is applied to the wrong channel. That the 13 ps loss remains the same for

all other wrong-channel combinations is not shown for simplicity reasons.

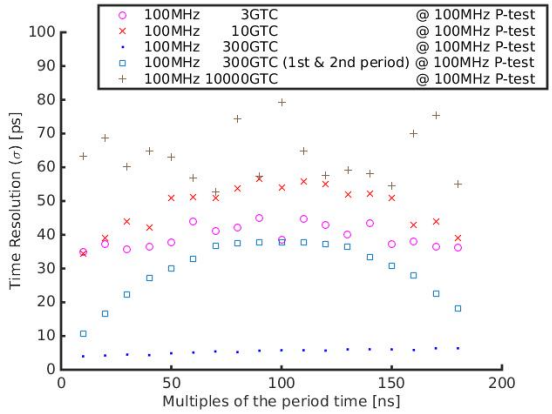
For better understanding the two individual parts of the LTC+3GTC are split and investigated with a 100 MHz P-test. First, the original LTC+3GTC is compared with the GTC as standalone TC-method but with varying iterations and correction ranges. The results of this P-test are provided in fig. 3.25. All standalone GTCs use an f_{TC}=100 MHz. The P-test in fig. 3.25(a) shows the time resolution (σ) vs. the delay when utilizing different GTCs and (b) illustrates its corresponding offsets. A maximum delay of two periods (1^{st} & 2^{nd} period) is only used in one case to perform the GTC corrections. The default settings (multiples of the period time $< \frac{3}{4} \cdot T_{SCA}$) are used in all other cases. Since the P-test histograms for 10000 iterations (10000GTC) did not match a Gaussian fit, the RMS values were calculated instead. The wrong TC outcome of the 10000GTC is shown in (c). The correct TC computed by the 300GTC can be found in (d) illustrating all 1024 Δt_b. It should be noticed that a unique Δt_b is negative which is Δt_{499}. $\Delta t_{499} = -7$ ps means that the signal that is stored in cell #498 arrived 7 ps later compared to the signal arrival in cell #499. In general only cell #498 shows this behavior for all tested DRS4s and only at fast sampling speeds.

The GTC does not require the f_{SCA} information of the DRS4 but rather delivers the f_{SCA}. Table 3.6 shows the f_{SCA} for the V3 that is measured with the GTC. The GTC measures the f_{SCA} with a certain error which is shown in fig. 3.27(f) and

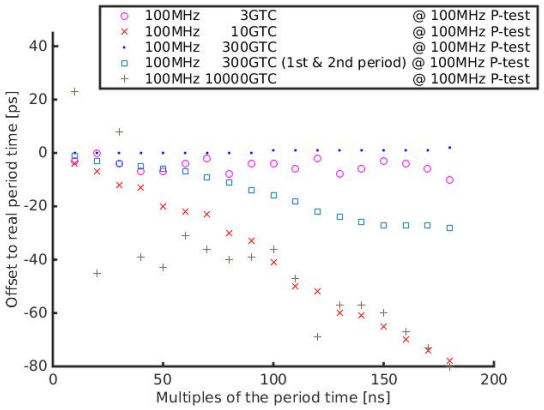
Table 3.6: Listed are the preset f_{SCA} and the true f_{SCA} of the V3. The two-state-effect divides the true f_{SCA} in two cases. Naturally, this is also the case for the preset T_{SCA} which is provided as T_{SCA} offset (left/right state).

f_{SCA} preset	true f_{SCA} left state	true f_{SCA} right state	expected T_{SCA} preset	T_{SCA} offset left/right state
5.12000 GHz	5.12065 GHz	5.12051 GHz	200,000 ps	-25 ps/-20 ps
1.98200 GHz	1.98220 GHz	1.98211 GHz	516,650 ps	-52 ps/-29 ps
1.00760 GHz	1.00736 GHz	1.00730 GHz	1,016,276 ps	242 ps/303 ps

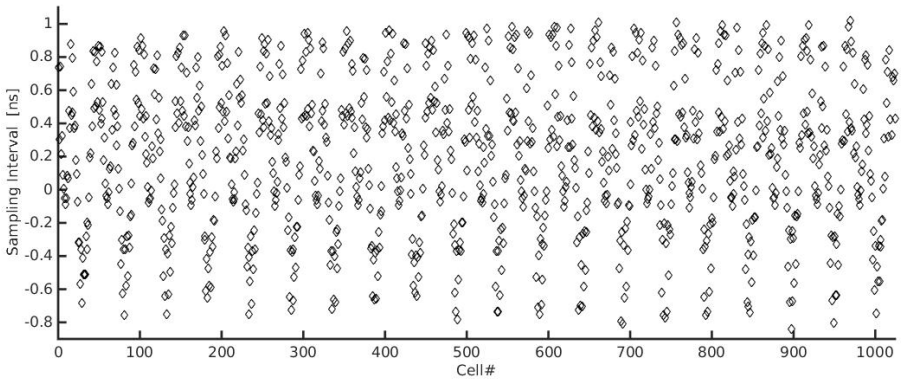
predicts an f_{SCA}=5.12065 GSPS.



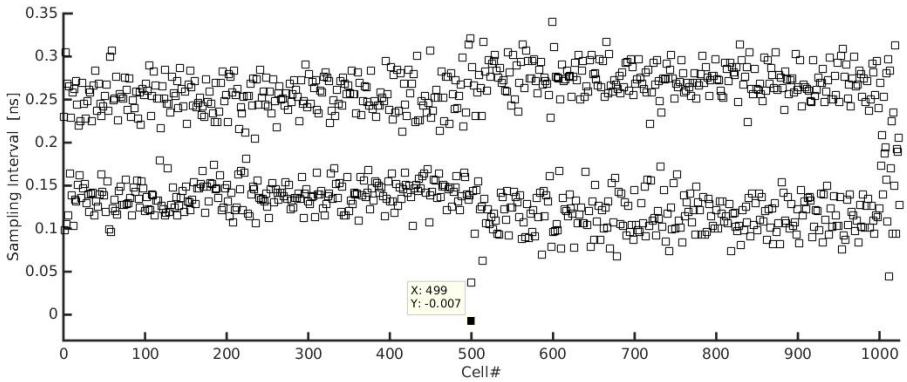
(a) σ values of 100 MHz P-test



(b) Offset of 100 MHz P-test



(c) All 1024 Δt_b from the GTC with 10000 iterations utilizing an f_{TC}=100 MHz

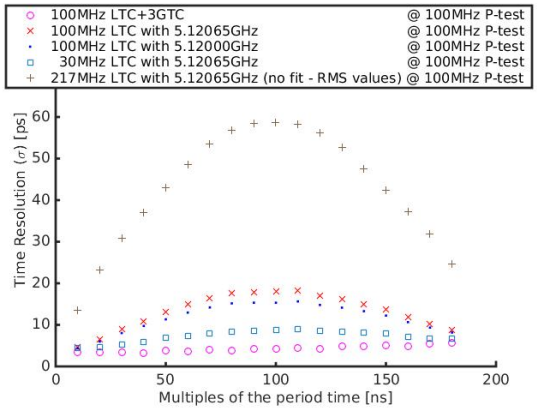


(d) All 1024 Δt_b from the GTC with 300 iterations (300GTC) utilizing an f_{TC}=100 MHz

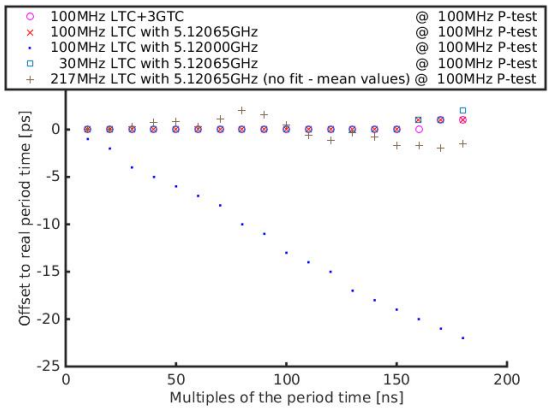
Figure 3.25: P-test when utilizing five cases of the standalone GTC (a & b). The f_{TC} and the test frequencies are 100 MHz. The curves in (a) show the σ values and their dedicated offsets can be found in (b). Additionally two GTC results demonstrate the set of 1024 Δt_b (e & f). The V3 is preset to 5.12 GSPS.

As illustrated in table 3.6, the wrong f_{SCA} is provided by the V3. The correct f_{SCA} is mandatory for the LTC which will be tested in the second part of

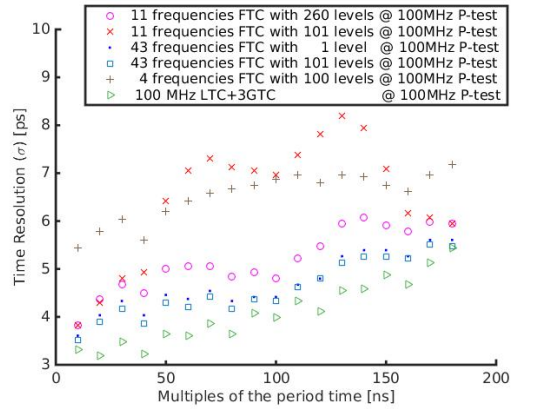
LTC+3GTC investigation. Its results are available in fig. 3.26(a & b) where P-tests are applied to the standalone LTCs. The P-tests also shows the results for the LTC



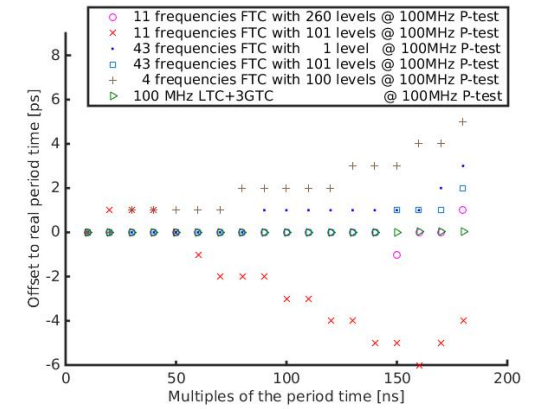
(a) σ values of P-test (NEW-TC vs. LTC)



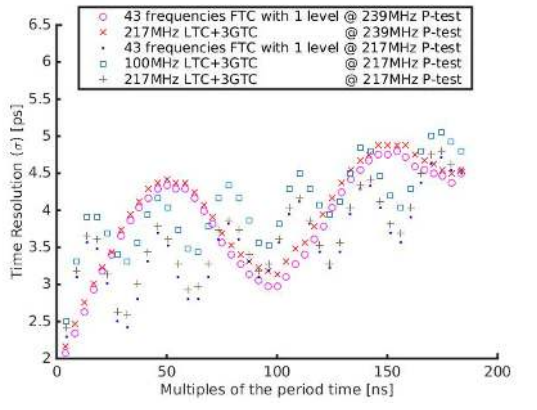
(b) Offset of P-test (NEW-TC vs. LTC)



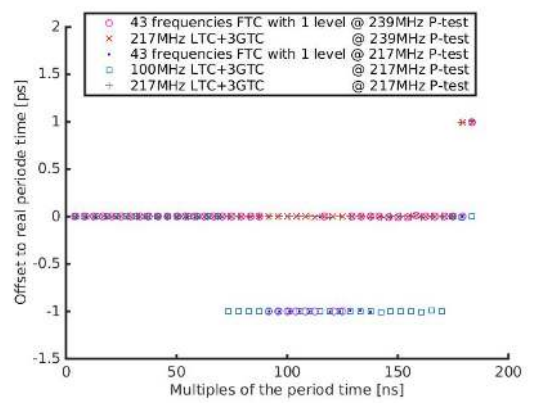
(c) σ values of P-test (NEW-TC vs. FTC)



(d) Offset of P-test (NEW-TC vs. FTC)



(e) σ values of fast frequency P-test



(f) Offset of fast frequency P-test

Figure 3.26: Three P-tests are shown analyzing the LTCs, FTCs and LTC+3GTCs. In each, five combinations are shown (see legend). In (a - d) the test frequency is 100MHz and in (e & f) more than 200 MHz. The plots on the left show the σ values. Their dedicated offsets can be found on the right. V3 is preset to 5.12 GSPS.

utilizing the corrected f_{SCA} vs. the wrong f_{SCA}. Again one will find the LTC+3GTC as the reference example. Further, the P-test includes a fast and a slow f_{TC} for the LTC. Additionally, four example histograms of the mentioned P-test can be found in fig. 3.27(a - d). One can see that the peak fit in (b) is shifted 13 ps compared to expected peak location in (a) caused by the wrong f_{SCA} information.

The P-test for different FTC settings[VII] is compared with the NEW-TC in the middle of fig. 3.26(c & d). The illustrated FTC settings are 43, 11 and 4 frequencies as visible in the legend of fig. 3.26(c & d). The FTC settings are also changed with respect to voltage levels. Another P-test compares three TC-methods in 5 combinations as shown at the bottom of fig. 3.26(e & f). The tested TC-methods are the FTC and two LTC+3GTCs with an f_{TC} of 217 MHz and 100 MHz. The applied P-test frequencies are 217 MHz and 239 MHz. One example histogram of the mentioned P-test is additionally illustrated in fig. 3.27(e).

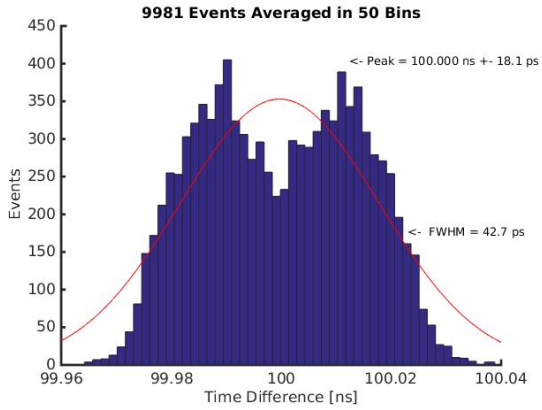
The comparison results of the most relevant NEW-TCs have been completed. Its

Table 3.7: Listed is the computing time of different NEW-TCs with a preset f_{SCA}=5.12 GSPS for the V3. Each digitized TC frequency consists of N_{wave}=1000. The FTC utilizes 43 frequencies. All other methods use a single TC frequency. The f_{TC} is 100 MHz for all GTCs including the LTC+3GTC. The performance of the P-test represents the time resolution of all first periods.

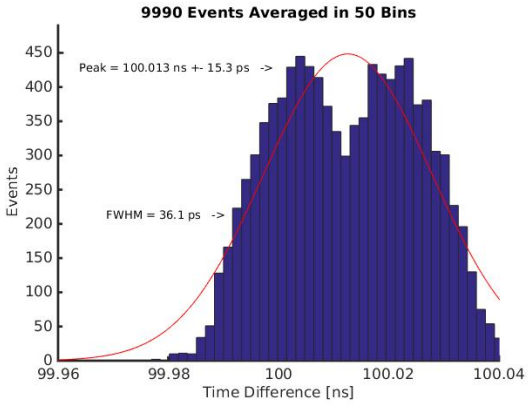
NEW-TC	computing time	100MHz P-test	details
43 frequencies FTC	47 seconds	≈3 ps	fig. 3.26(c)
30 MHz LTC	3.7 seconds	≈5 ps	fig. 3.26(a)
3GTC	1.2 seconds	≈30 ps	fig. 3.25(a)
10GTC	4.0 seconds	≈30 ps	fig. 3.25(a)
300GTC	2.0 minutes	≈3 ps	fig. 3.25(a)
10000GTC	66 minutes	≈70 ps	fig. 3.25(a)
LTC+3GTC	4.9 seconds	≈3 ps	fig. 3.24(a)

processing times are summarized in table 3.7 including its general TC performance.

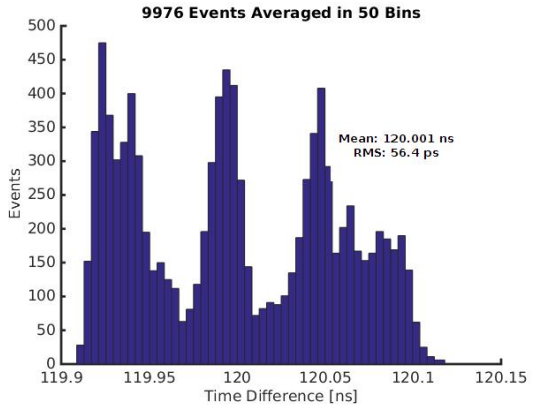
[VII] The 43 frequencies FTC with 1 level is the first successful working NEW-TCs of this thesis. The theory is described in section 2.2.2 and the labeling is explained in section 2.2.7



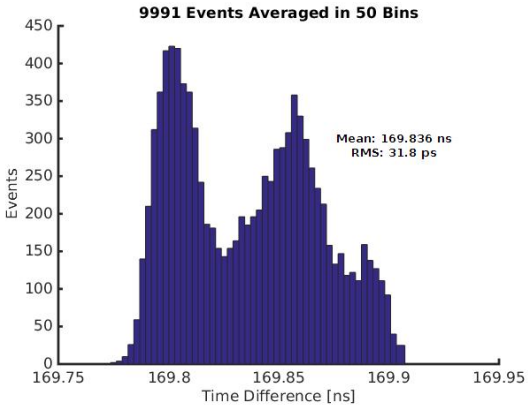
(a) 100MHz LTC with 5.12065GHz @ 10^{th} period (100MHz)



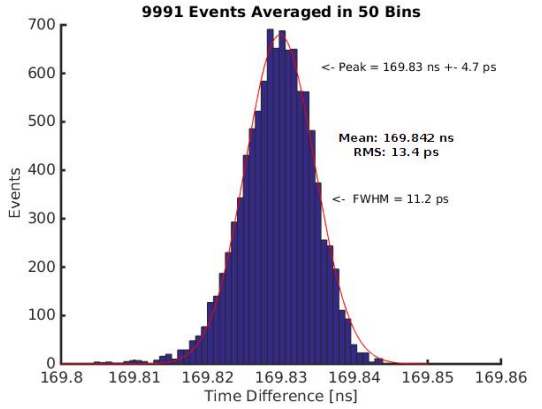
(b) 100MHz LTC with 5.12000GHz @ 10^{th} period (100MHz)



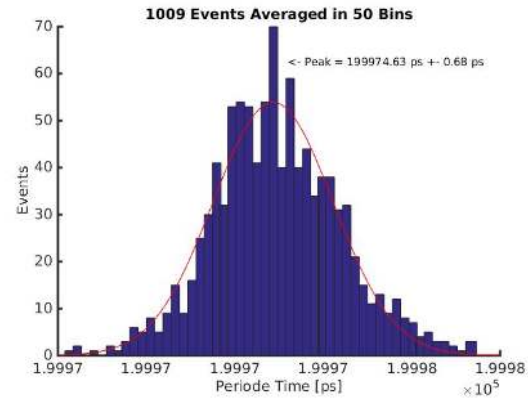
(c) 217MHz LTC with 5.12065GHz @ 12^{nd} period (100MHz)



(d) 217MHz LTC with 5.12065GHz @ 37^{th} period (239MHz)

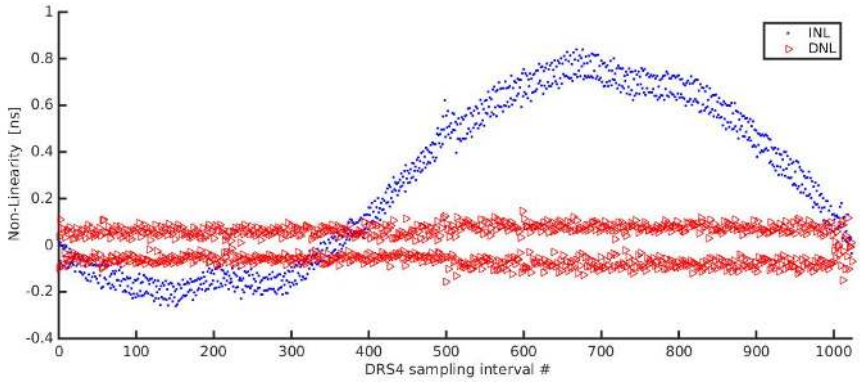


(e) 217MHz LTC+3GTC @ 37^{th} period (239MHz)

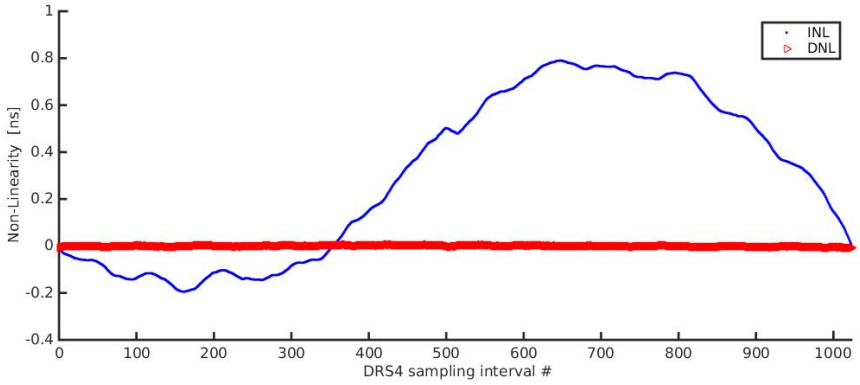


(f) Period time distribution for 20 °C

Figure 3.27: The P-tests in (a - e) show the time resolution histograms for five combinations of test frequencies and NEW-TCs. The test frequency is labeled in brackets. (f) shows the GTC fluctuation. V3 is preset to 5.12 GSPS in all plots.



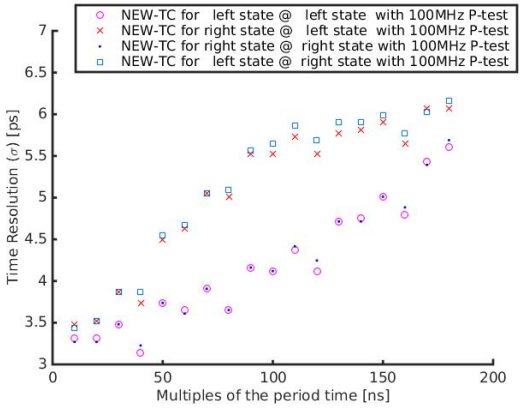
(a) NEW-TC outcome (INL and DNL) when the DRS4 is running at 5.12 GSPS



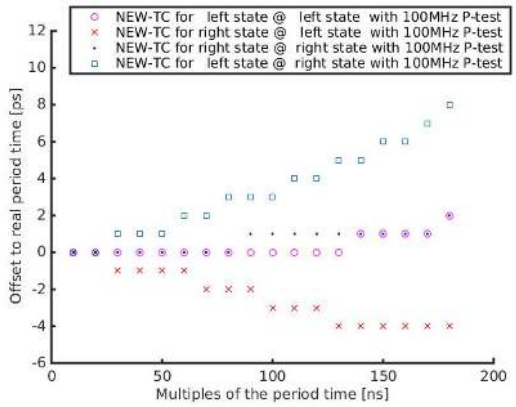
(b) V3-TC outcome (INL and DNL) when the DRS4 is running at 5.12 GSPS

Figure 3.28: Illustrated are the INL and DNL of the sampling intervals resulting from the NEW-TC (a) and the V3-TC (b). The V3 is preset to 5.12 GSPS.

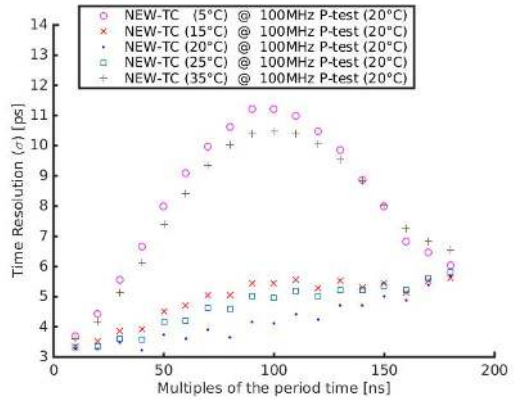
The TC outcome of the NEW-TC for the V3 follows in fig. 3.28. It shows the INL and DNL behavior of the NEW-TC in comparison to the V3-TC. The DNL in fig. 3.28(a) is equivalent to the set of 1024 Δt_b in fig. 3.25(d) with the difference that the DNL illustrates the subtraction from the expected sampling intervals. Thus, the DNL only results in a horizontal zero curve like in fig. 3.28(b) if all 1024 Δt_b have the same value. The corresponding INL will result in the zero curve if the sum of Δt_b creates a time line as 0 ps, 200 ps, 400 ps, and so forth (f_{SCA}=5 GSPS). One can see that both behaviors of the associated curves in fig. 3.28 look similar for both TC-methods with the difference that the alternating character which results in two distinguishable curves is missing for the V3-TC. The alternating behavior results in an increased standard deviation when averaging the set of Δt_b ($\Delta \bar{t}_b$) as shown in table 3.8.



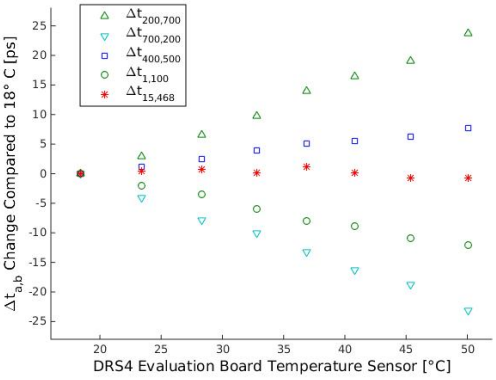
(a) σ values of P-test (two-state-effect)



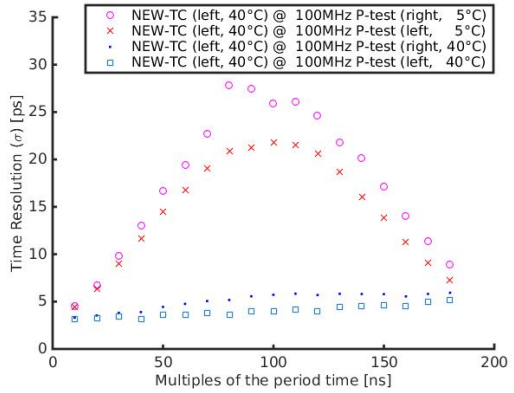
(b) Offset of P-test (two-state-effect)



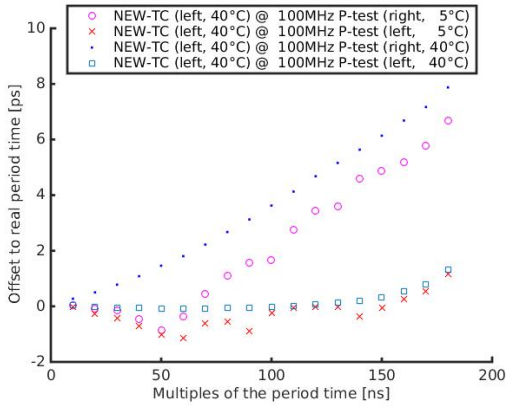
(c) σ values of P-test (20 °C vs. 5-35 °C)



(d) $\Delta t_{a,b}$ vs. temperature



(e) σ values of P-test (5 °C vs. 40 °C)



(f) Offset of P-test (5 °C vs. 40 °C)

Figure 3.29: Three P-tests analyzing the two-state-effect, the temperature influence and the combination of both when utilizing the NEW-TC. The plots on the left show the σ values. Two dedicated offsets can be found on the right (b & f). The two-state-effect scenario is labeled with "right" or "left". The test frequency is 100 MHz for all P-tests. (d) shows the temperature dependency of the V3 for five cases. V3 is preset to 5.12 GSPS for all measurements.

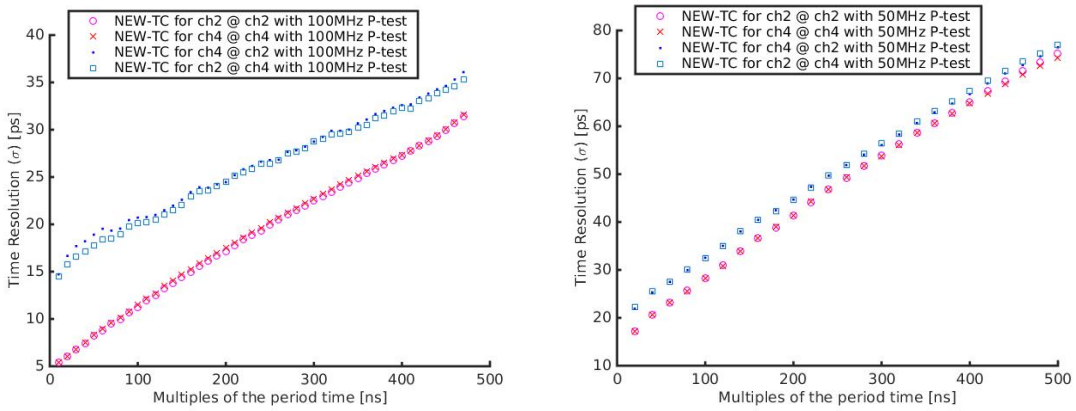
Table 3.8: Listed from the 2nd to the 5th column is the mean sampling interval ($\Delta\bar{t}_b$) and its fluctuation (± RMS). The $\Delta\bar{t}_b$ is provided for three f_{SCA} when utilizing two different TC-methods. Column #2 lists the $\Delta\bar{t}_b$ resulting from the V3-TC. In contrast one will find the correct $\Delta\bar{t}_b$ from the NEW-TC in column #3. Further, in column #4 & 5 the correct $\Delta\bar{t}_b$ is separated in odd and even cells. In the last column its extrema are available which provide the shortest and the longest measured Δt_b as experienced from 30 calibrated DRS4-chips.

preset f_{SCA}	V3-TC	NEW-TC	even $\Delta\bar{t}_b$	odd $\Delta\bar{t}_b$	extrema
5.1200 GHz	195±3 ps	195±72 ps	264±22 ps	127±21 ps	-20−390ps
1.9820 GHz	505±8 ps	504±122 ps	612±54 ps	397±59 ps	0.2−0.8 ns
1.0076 GHz	993±30ps	993±228 ps	1034±217ps	952±234ps	0.2−1.8 ns

The last three P-tests of this sub-section are illustrated in fig. 3.29. All these P-tests use the TC outcome resulting from the LTC+3GTC with f_{TC}=100 MHz which is labeled as NEW-TC. The test frequency is also 100 MHz for all P-tests. Fig. 3.29(a & b) shows the P-test of all two-state-effect combinations. (c) shows the temperature dependency of the DRS4 and (e & f) the combination of both, two-state-effect and temperature. The $\Delta t_{a,b}$ change over temperature for five chosen cases are additionally visualized in (d). Five $\Delta t_{a,b}$ drifts were measured at 8 different temperature levels (see table 3.5). The 5 drifts were calculated by subtracting the $\Delta t_{a,b}$ from its corresponding 18 °C case.

3.3.2 P-Test at 1GSPS and 2GSPS

A channel dependent TC for 2 GSPS and 1 GSPS is shown in fig. 3.30. Both plots show the time resolution (σ) up-to a delay of ≈500 ns. The four combinations of channel #2 and channel #4 are shown in each plot.

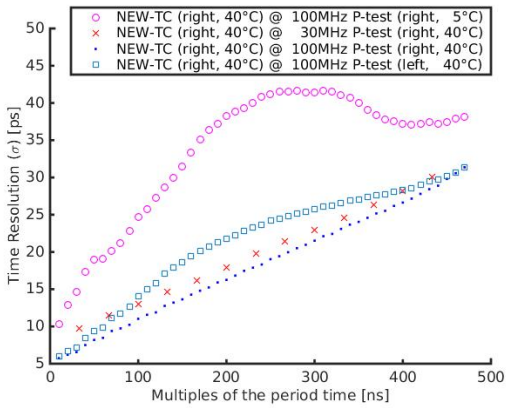


(a) P-test for 2 GSPS with 100 MHz **(b)** P-test for 1 GSPS with 50 MHz

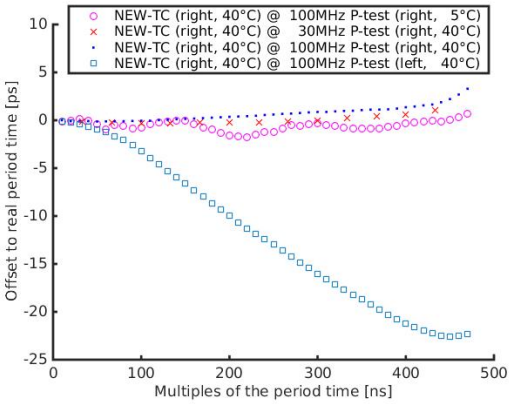
Figure 3.30: Two P-tests of the V3 testing the channel dependency when utilizing the NEW-TC. The plots show the time resolution for two f_{SCA} (1 GSPS and 2 GSPS). In each, four channel combinations are shown (see legend).

The temperature and other setting changes have been additionally investigated for 1 GSPS and 2 GSPS. The results of the P-test for the 2 GSPS measurement can be found in fig. 3.31(a & b). The plot on the left shows the time resolution (σ) vs. the delay. On the other side one will find their corresponding offsets. One can see that the applied NEW-TC belongs to the right state with an environmental temperature of 40°C. Further, two temperatures, both states and two test frequencies have been applied for this P-test. Fig. 3.31(c) illustrates the INL and DNL of the NEW-TC outcome and fig. 3.31(d) the dedicated V3-TC outcome when sampling at 2 GSPS. The correct sampling frequency can be found in table 3.6.

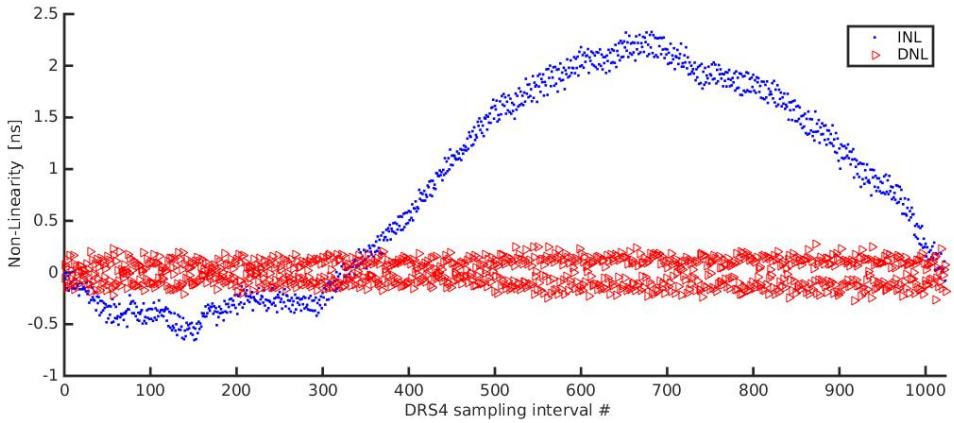
The results of the P-test for 1 GSPS is given in fig. 3.32(a & b). The NEW-TC utilizes an f_{TC} of 100 MHz collected at 5°C for the right state. The applied P-test investigates two temperatures, both states and two test frequencies. Fig. 3.32(c) illustrates the INL and DNL of the NEW-TC outcome and fig. 3.31(d) the dedicated V3-TC outcome when sampling at 1 GSPS. The correct sampling frequency can be found in table 3.6.



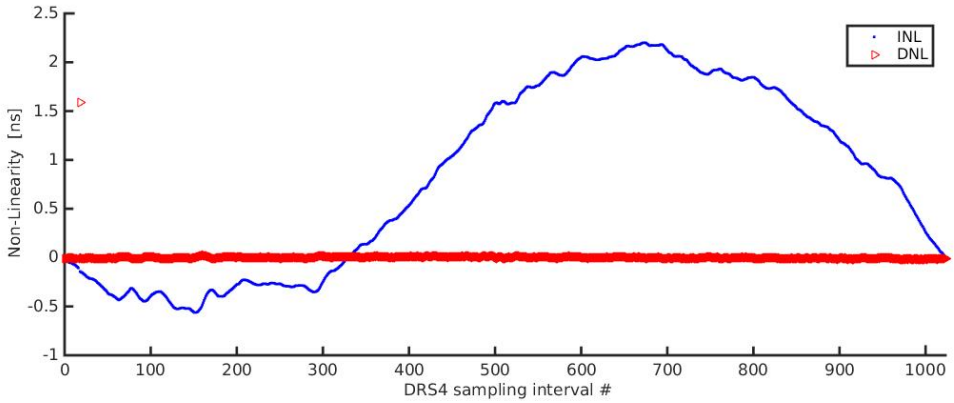
(a) σ values of P-test



(b) Offset of P-test

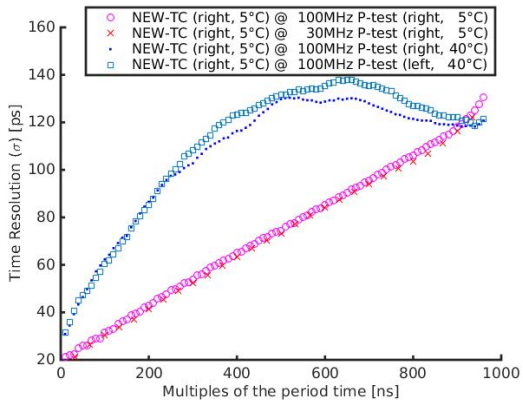


(c) NEW-TC outcome (INL and DNL) when the DRS4 is running at 2 GSPS

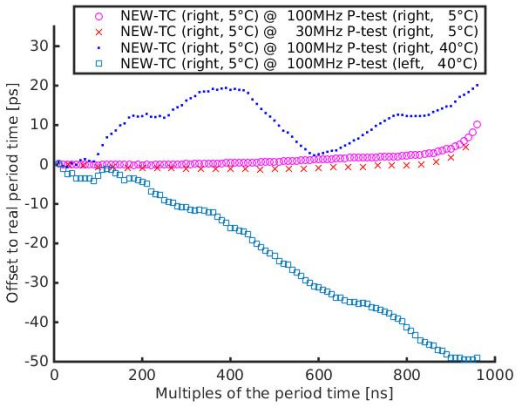


(d) V3-TC outcome (INL and DNL) when the DRS4 is running at 2 GSPS

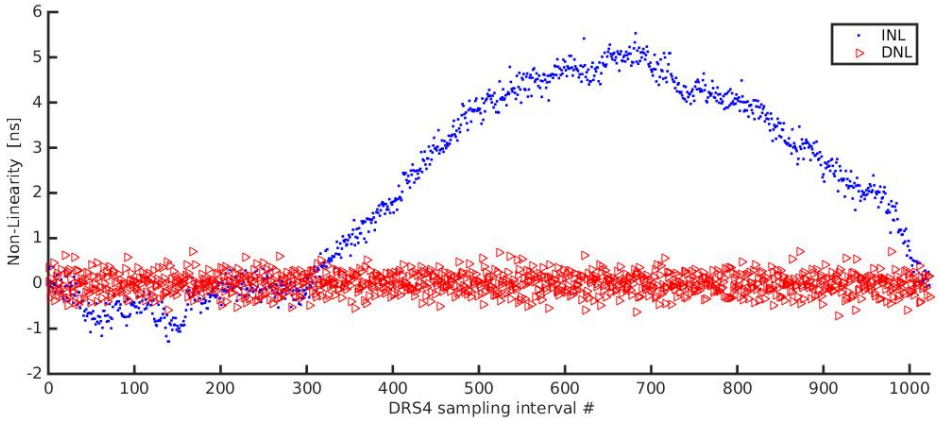
Figure 3.31: P-test analyzing the two-state-effect and the temperature influence with the NEW-TC. The two-state-effect scenario is labeled with "right" or "left". Four combinations are shown (see legend). (a) shows the time resolution (σ) vs. the delay. (b) illustrates its corresponding offsets. In (c) one will find the outcome of the NEW-TC and in (d) the outcome of the V3-TC. The V3 is preset to 2 GSPS for all measurements.



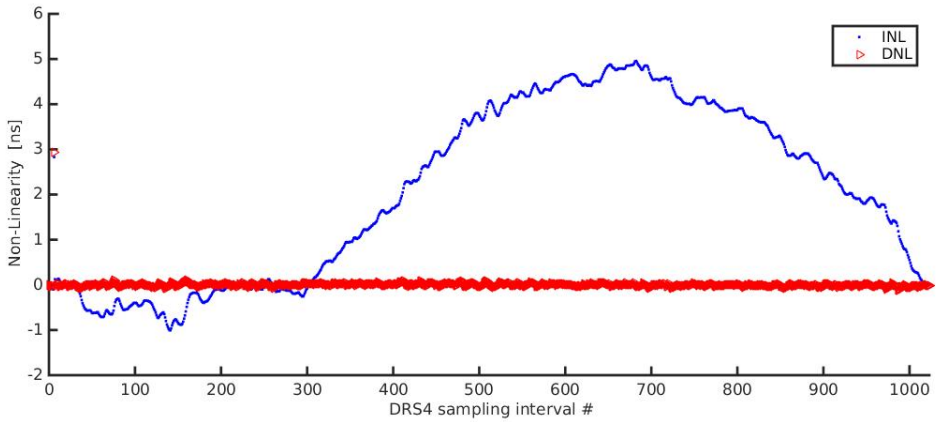
(a) σ values of P-test



(b) Offset of P-test



(c) NEW-TC outcome (INL and DNL) when the DRS4 is running at 1 GSPS

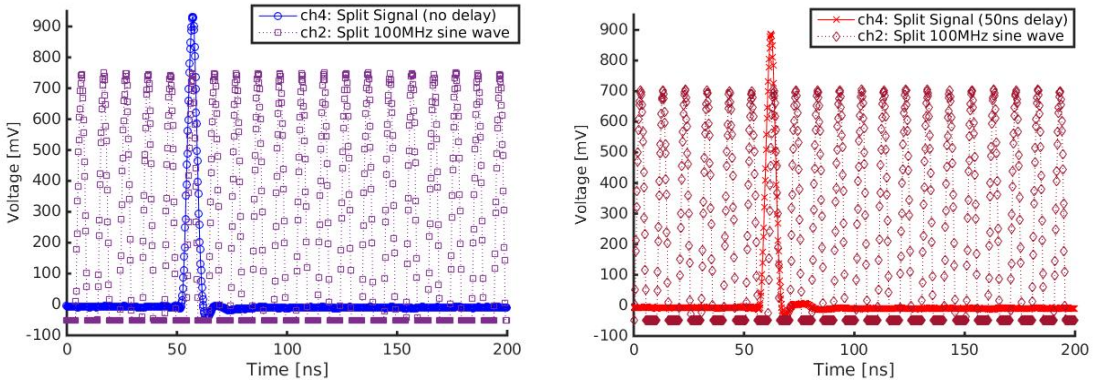


(d) V3-TC outcome (INL and DNL) when the DRS4 is running at 1 GSPS

Figure 3.32: P-test analyzing the two-state-effect and the temperature influence with the NEW-TC. The two-state-effect scenario is labeled with "right" or "left". Four combinations are shown (see legend). (a) shows the time resolution (σ) vs. the delay. (b) illustrates its corresponding offsets. In (c) one will find the outcome of the NEW-TC and in (d) the outcome of the V3-TC. The V3 is preset to 1 GSPS for all measurements.

3.3.3 SP-Test

This SP-test is separated into two cases. The first case tests a single DRS4-chip and the second case two independent running DRS4-based boards. The boards are preset to f_{SCA}=5.12 GSPS for all SP-tests. More experimental details are available in section 2.5.2.

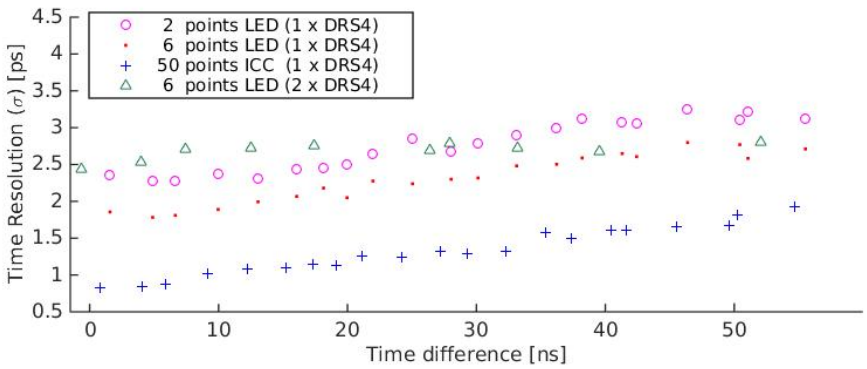


(a) V5 **(b)** V3

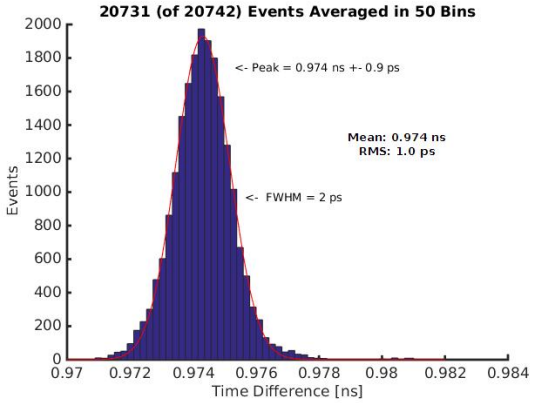
Figure 3.33: Illustrated in (a) and (b) is an example event of an SP-test between V3 and V5. For each board two channels are displayed. In channel # 2 (ch2) one can see the digitized split sine wave and in channel # 4 (ch4) the split pulse. In the given example the waveform is stooped at c_{stop}= 24 for V3 and triggered at c_{stop}= 874 for V5. Both boards are preset to 5.12 GSPS.

An event of the single-DRS4-chip case looks identical to the two-DRS4-chips case with the difference that no reference clock is needed. The single-DRS4-chip SP-test utilizes channels #2 and channels #4 of the V3 (NEW-TC). A single event of the two-DRS4-chips case is available in fig. 3.33. The split pulse is shown by both channels #4 (ch4) and the split reference clock is digitized by both channels #2 (ch2). The trigger rate is preset below 1 Hz, since the two independent running DRS4-based boards do not have a global trigger. This guarantees that all digitized waveforms of the first board belong to corresponding waveforms of the second board. The V5 is used as the second DRS4-based board because only one V3 is available. Although the V5 already utilizes an improved TC, which is strongly influenced by this thesis, the V5 is calibrated identically to the V3 to guarantee equal board conditions. The results of the NEW-TC applied to the V5 can be found in section 3.5.1.

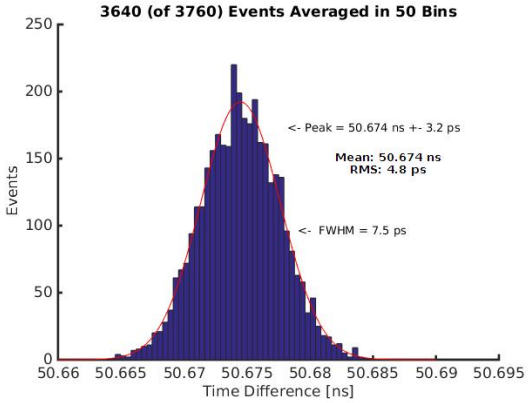
Fig. 3.34(a) shows the SP-test results for both, the single-DRS4-chip case and



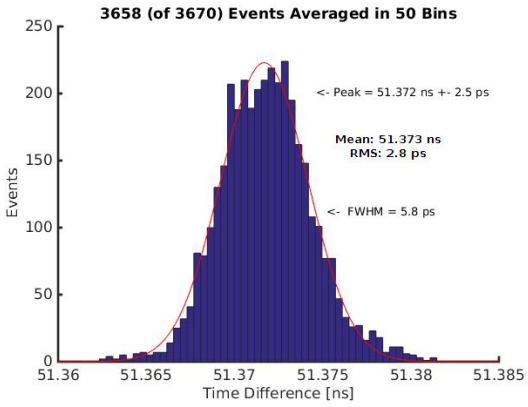
(a) SP-test



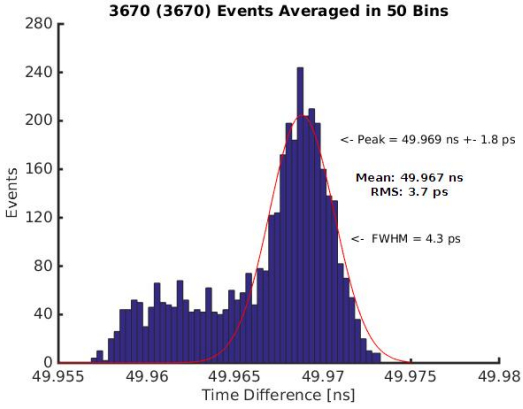
(b) 50 points ICC (1 ns delay)



(c) 2 points LED (50 ns delay)

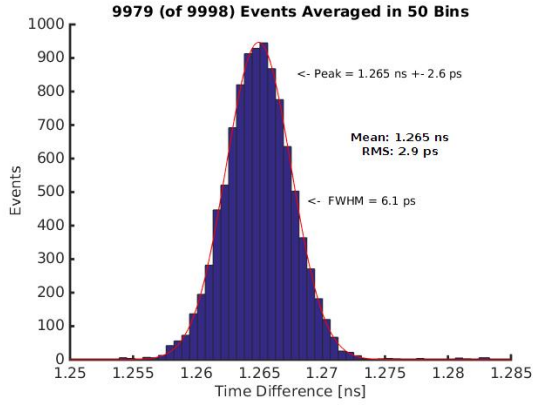


(d) 6 points LED (50 ns delay)

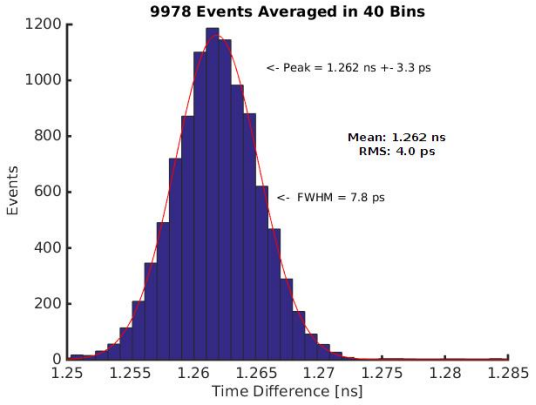


(e) 50 points ICC (50 ns delay)

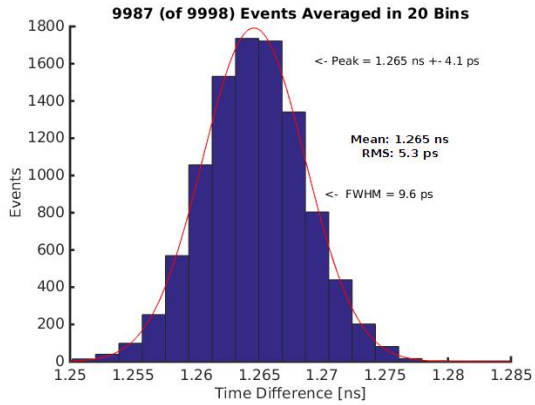
Figure 3.34: In (a) the SP-test measurements with the V3 and the V5 when applying the NEW-TC are shown. The triangles show the SP-test results of two independently running boards, where a 6-points LED is used. For the other 3 curves, the SP-test is performed with the V3, where the same dataset is analyzed three times using different analyzing techniques. In (b – e) one will find four histogram examples of the $1 \times$ DRS4 SP-tests.



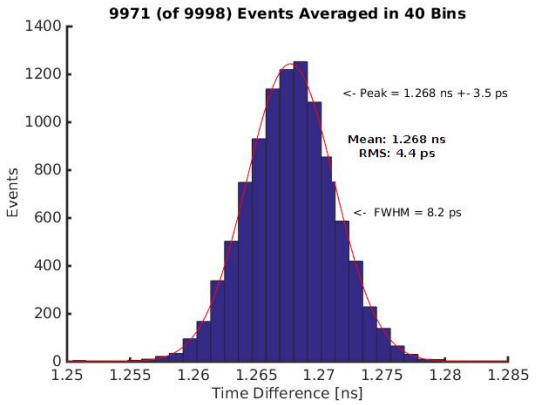
(a) 6 points for all LEDs



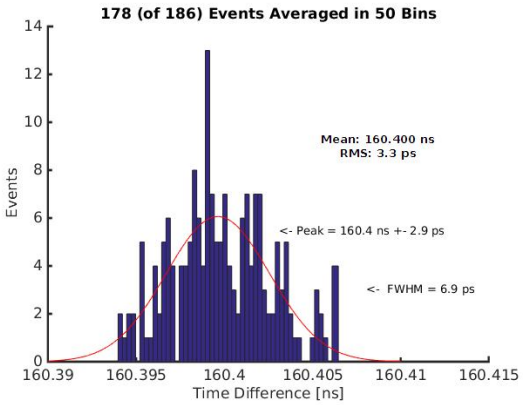
(b) 2 points for split pulse, other LEDs 6 points



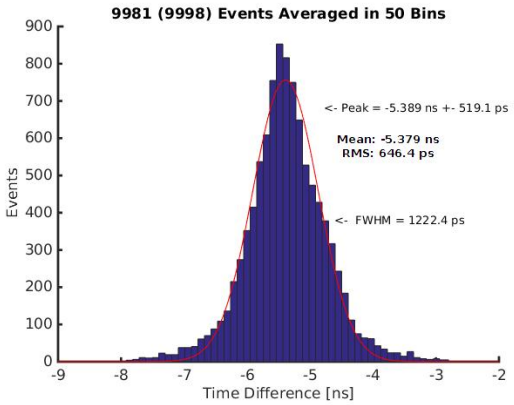
(c) 2 points for all LEDs



(d) 6 points for split pulse, other LEDs 2 points



(e) 6 points for all LEDs and 160 ns delay



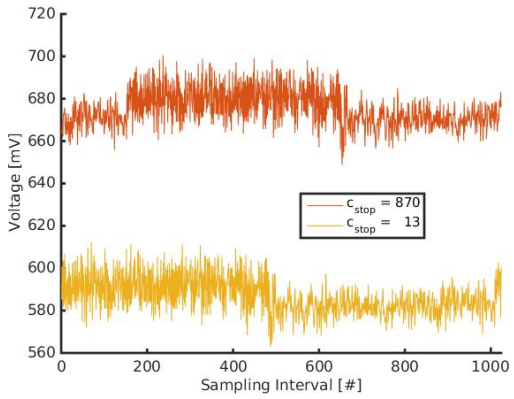
(f) Jitter between V3 and V5

Figure 3.35: Six SP-test histograms are shown from the two-DRS4-chips case ($2 \times$ DRS4). Histogram (a) presents the second data point of fig. 3.34(a). The dedicated curves of the three histograms (b – d) are not shown in fig. 3.34 but illustrate the time resolution change for (a) when modifying the LED settings. (e) shows the worst case scenario of the SP-test with a 6-points LED where the trigger delay of the second board is intentionally set to 160 ns. (f) illustrates the time jitter between the two free running boards.

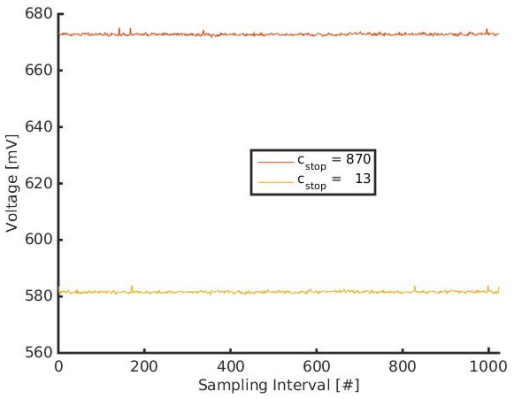
the two-DRS4-chips case. The LED (2 SPs and 6 SPs) and the ICC (50 SPs) are the two analyzing techniques used for the SP-tests. The following figures 3.34(b - e) are four example histograms extracted from the single-DRS4-chip case ($1 \times$ DRS4). The histogram in fig. 3.34(e) shows no perfect Gaussian distribution which starts getting visible at around 30 ns delay.

All six example histograms in fig. 3.35 refer to the two-DRS4-chips case. The histogram outcome in fig. 3.35(a) stands for the second data point in fig. 3.34 ($2 \times$ DRS4). The other histograms in fig. 3.35(b – d) show the performance change of the same data point if the LED settings are modified. Further, the histogram in fig. 3.35(e) illustrates the time resolution for a delay of 160 ns and histogram (f) gives an idea of the global trigger jitter of two independently running DRS4-chips.

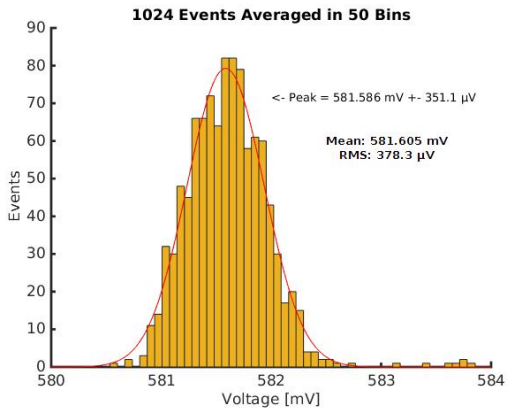
3.4 X742 when Utilizing new Calibrations



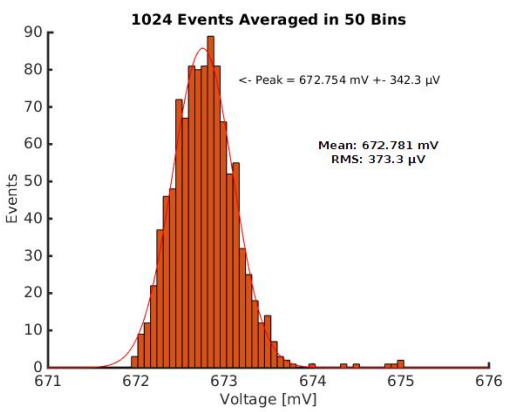
(a) Two baseline waveforms with NO-VC



(b) Two baseline waveforms with NEW-VC



(c) Noise spectrum of c_{stop}=13

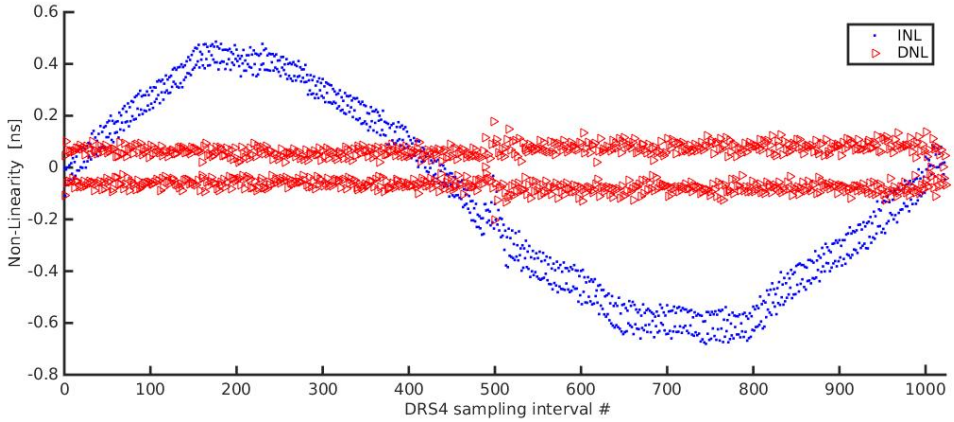


(d) Noise spectrum of c_{stop}=870

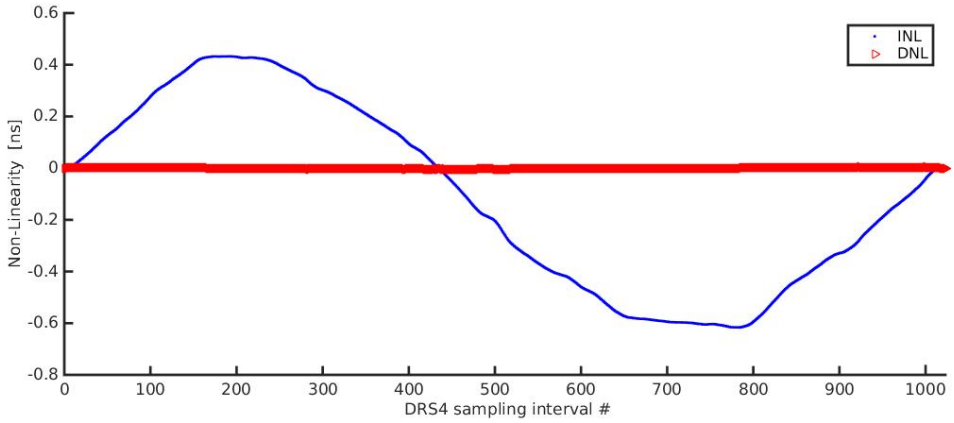
Figure 3.36: All figures show the baseline noise of all 1024 SPs for channel #4 when sampling at 5 GSPS. In (a) and (b) all 1024 SP are plotted over time for two c_{stop} scenarios with and without VC. The histograms in (c) and (d) illustrate both c_{stop} scenarios with the NEW-VC.

The results of the DT5742 when applying the new calibration techniques can be found in this section. Only the results for f_{SCA} equal to 5 GSPS will be shown. Other f_{SCA} results for the DRS4-chip are available in section 3.3.2.

The first baseline measurements with an input trigger rate of 1 kHz were performed to investigate the NEW-VC. In total 1000 waveforms were digitized for this VC. Although, two c_{stop} are theoretically enough for the NEW-VC, all 24 c_{stop} were fed to the NEW-VC algorithm. Only the first 800 SPs were found stable when sampling with the X742. Thus, at least 3 c_{stop} scenarios are mandatory for a success-



(a) NEW-TC



(b) CAEN-TC

Figure 3.37: In (a) one will find the INL and the DNL for an ideal-calibrated X742 and in (b) the corresponding CAEN-TC when running at 5 GSPS.

ful NEW-VC. Two NEW-VC examples when sampling at 5 GSPS are available in fig. 3.36. One can see if the NEW-VC is executed successfully, the resulting baseline noise will be around 0.35 mV (σ).

Afterwards, the NEW-TC was utilized. The corresponding results between the original sampling intervals (CAEN -TC) and the NEW-TC are available in fig. 3.37 for 5 GSPS. The other sampling speeds are summarized in table 3.9.

The P-test and SP-test results are not shown because they are identically to the V3-results of section 3.3.1. The time jitter when triggering two DRS4-chips of the same X742 was measured to be around 30 ps (σ).

The PET-results for PMTs and SiPMs coupled to various scintillator crystals are found in the following three sub-sections. All SiPM measurements utilize a digital

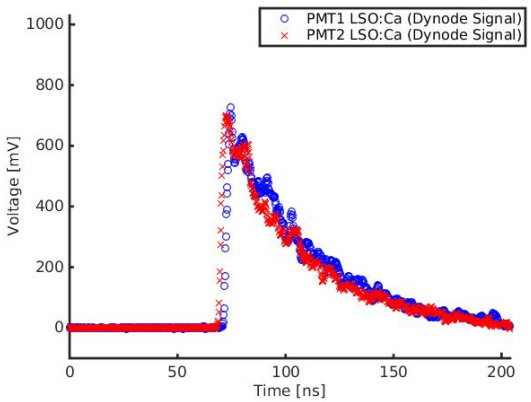
Table 3.9: Listed from the 2nd to the 5th column is the mean sampling interval ($\Delta\bar{t}_b$) and its fluctuation (± RMS). The $\Delta\bar{t}_b$ is provided for three f_{SCA} when utilizing two different TC-methods. Column #2 lists the $\Delta\bar{t}_b$ resulting from the CAEN-TC. In contrast one will find the correct $\Delta\bar{t}_b$ from the NEW-TC in column #3. Further, in column #4 & 5 the correct $\Delta\bar{t}_b$ is separated in odd and even cells. In the last column its extrema are available which provide the shortest and the longest measured Δt_b as experienced from 30 calibrated DRS4-chips.

preset f_{SCA}	CAEN-TC	NEW-TC	even $\Delta\bar{t}_b$	odd $\Delta\bar{t}_b$	extrema
5.0000 GHz	200±3 ps	200±74 ps	270±23 ps	130±23 ps	-15−400ps
2.5000 GHz	400±7 ps	400±102 ps	493±43 ps	307±42 ps	0.1−0.7 ns
1.0000 GHz	1000±31ps	1000±230ps	1036±225ps	965±227ps	0.2−1.8 ns

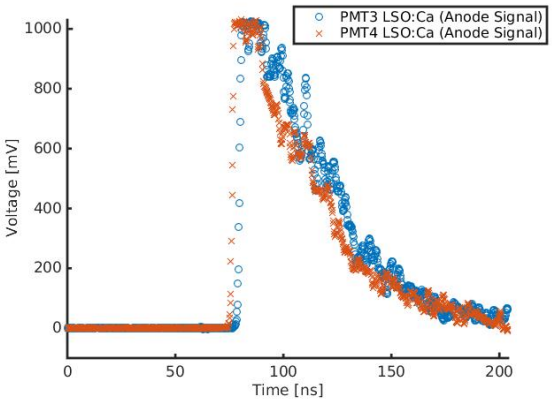
LED (2-points interpolation) with no additional corrections. The PMT measurements have been analyzed equally but with a walk correction.

3.4.1 CRT-Test with PMTs Coupled to LSO:Ca

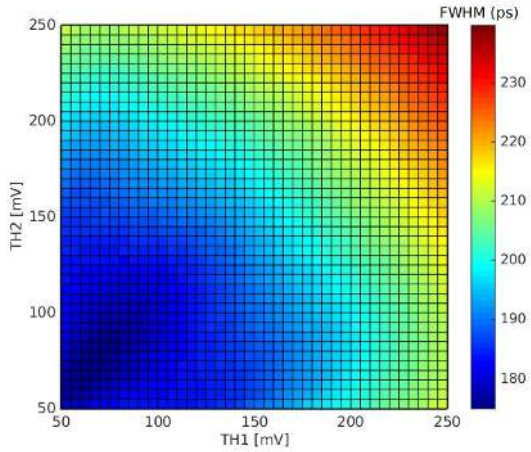
A similar measurement as illustrated in section 3.2.3 is demonstrated in this subsection. This CRT-test provides a delay case of 50 cm and again only energies inside the photo-peak are used. Additionally both, anode and dynode signals are analyzed utilizing the new calibration methods (CAEN-VC and CAEN-TC). The amplitude of the anode is approximately double the height of the dynode output as illustrated in fig. 3.38(a & b) . Although the NEW-VC is applied, the $\frac{\Delta E}{E}$ of the dynode is identical to fig. 3.22 in section 3.2.3 and therefore not illustrated again. The time resolution results for a digital LED (2-points lin. fit) are found in fig. 3.38 and the outcome of the walk corrected LED (2-points lin. fit) are available in fig. 3.39. The anode signal exceeds the dynamic range of the X742 which is around 1.06 V. Therefore, the walk correction for the anode signal is made, by using the energy information of the dynode signal.



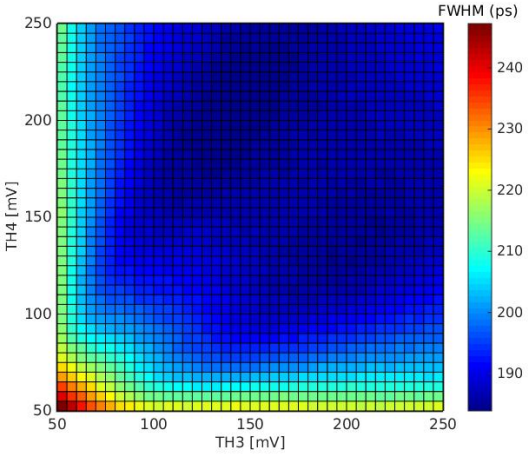
(a) Digitized coincident dynode event



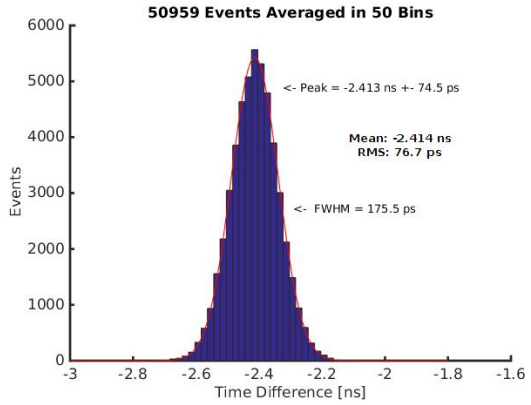
(b) Digitized coincident anode event



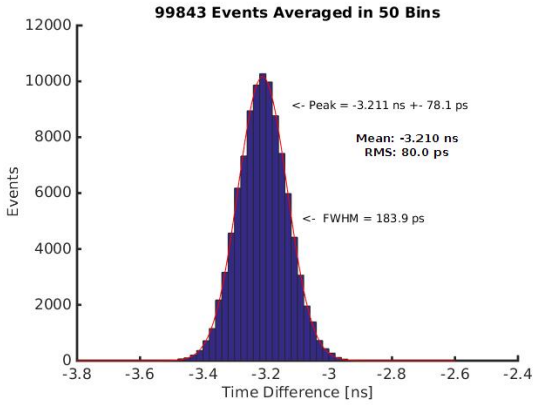
(c) CRT-test for dynode



(d) CRT-test for anode

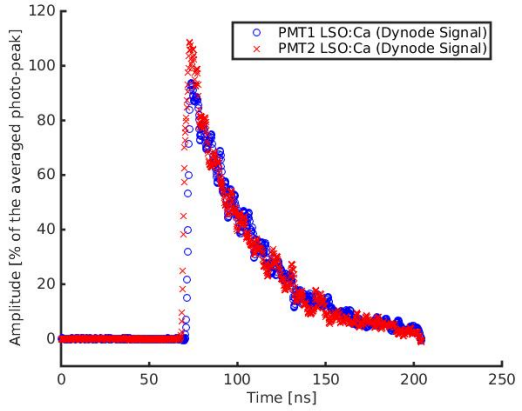


(e) Best THs for dynode

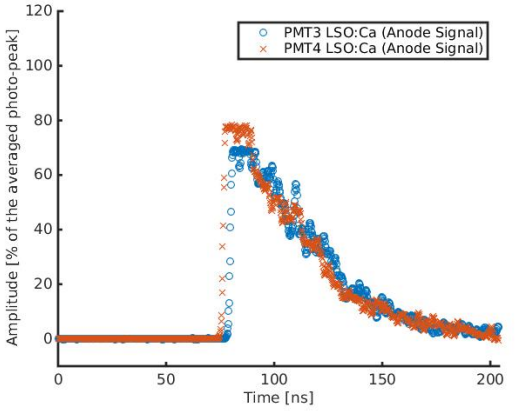


(f) Best THs for anode

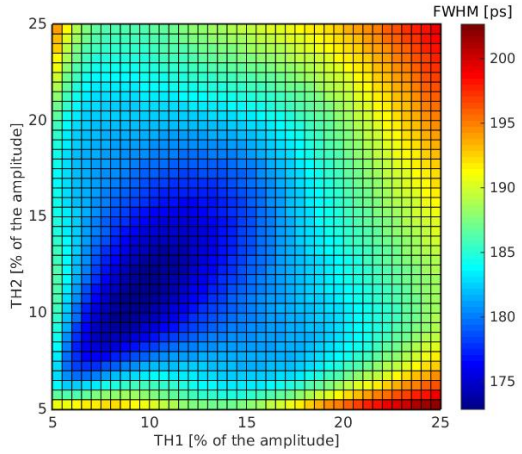
Figure 3.38: Shown are two CRT-tests with PMTs when utilizing the DT5742 at 5 GSPS (no walk correction). The left side shows the dynode results and the right side the anode outcome. (a & b) show a single digitized coincident PET-event example. The CRT-test in (c) and (d) show the time resolution (FWHM) vs. THs when utilizing the NEW-TC. (e) and (f) illustrates the measured histogram of the points with the best timing resolution, which is 65 mV (TH1), 70 mV (TH2), 140 mV (TH3) and 210 mV (TH4).



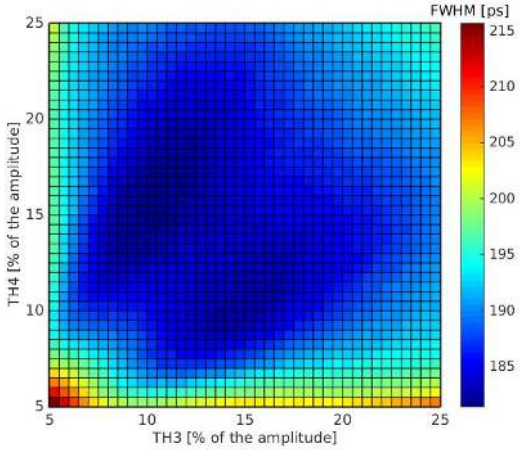
(a) Normalized dynode event



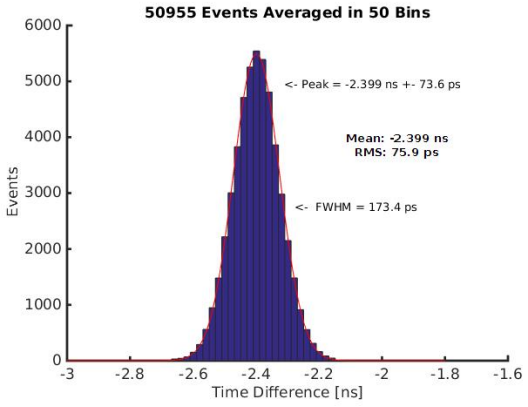
(b) Normalized anode event



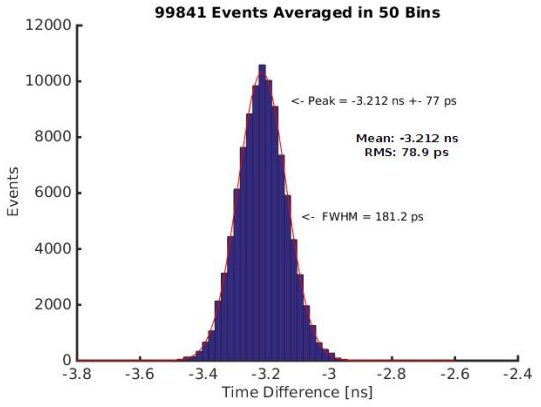
(c) CRT-test for dynode



(d) CRT-test for anode



(e) Best THs for dynode



(f) Best THs for anode

Figure 3.39: Shown are two CRT-tests with PMTs when utilizing the DT5742 at 5 GSPS (with walk correction). The left side shows the dynode results and the right side the anode outcome. (a & b) show a single digitized coincident PET-event example. The CRT-test in (c) and (d) show the time resolution (FWHM) vs. both normalized THs when utilizing the NEW-TC. (e) and (f) illustrate the measured histogram of the point with the best timing resolution, which is 9 % (TH1), 10.5 % (TH2), 10 % (TH3) and 15 % (TH4).

3.4.2 CRT-Tests for Calibrating the Reference PMT

The reference PMT for the following MPPC measurements in section 3.4.3 will be calibrated in this sub-section. To calibrate the reference PMT three CRT-tests are performed. The reference PMT and two identical SiPMs (SiPM1 & SiPM2) coupled to LSO are utilized with the DT5742 (NEW-TC) for this purpose. Details concerning the reference PMT and the SiPM-detectors are available in section 2.5.5.

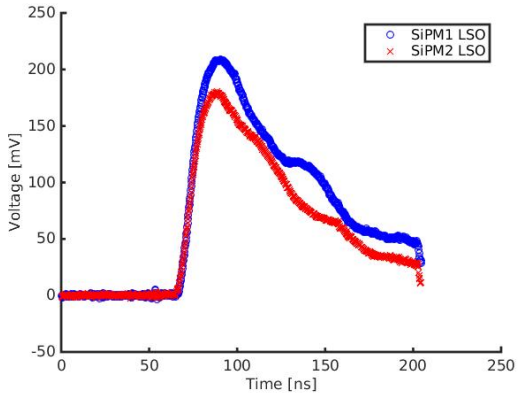
SiPM1, SiPM2, and reference PMT refer to TH-setting TH1, TH2, and TH3 respectively. A digital LED is used (2-points linear interpolation) for the CRT-test. A walk correction is only applied for the reference PMT by normalizing the waveform with the averaged photo-peak information. Energies inside the Compton continuum are not considered for the CRT. The results of the CRT-test between SiPM1 and SiPM2 can be found in fig. 3.40. The CRT-test between SiPM1 and the reference PMT are illustrated in fig. 3.41 and between SiPM2 and the reference PMT in fig. 3.42. The outcome of the three CRT-tests when applying (2.34) result in

$$\begin{aligned}\sqrt{\sigma_{SiPM1}^2 + \sigma_{SiPM2}^2} &= 560\,\text{ps (FWHM)}\\ \sqrt{\sigma_{PMT3}^2 + \sigma_{SiPM1}^2} &= 607\,\text{ps (FWHM)}\\ \sqrt{\sigma_{SiPM2}^2 + \sigma_{PMT3}^2} &= 551\,\text{ps (FWHM)}\end{aligned} \tag{3.1}$$

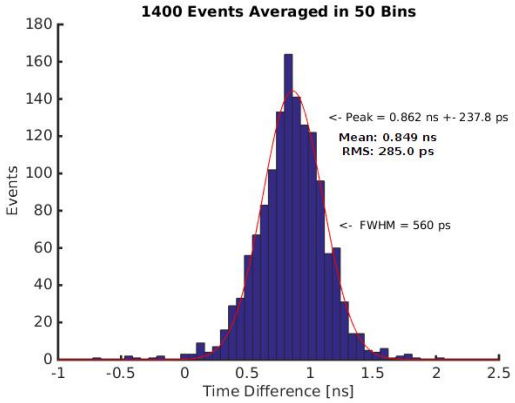
The single time resolution of the individual detectors can be calculated by solving (3.1) and results in (3.2).

$$\begin{aligned}\sigma_{SiPM1} &= 435\,\text{ps (FWHM)}\\ \sigma_{SiPM2} &= 353\,\text{ps (FWHM)}\\ \sigma_{PMT3} &= 423\,\text{ps (FWHM)}\end{aligned} \tag{3.2}$$

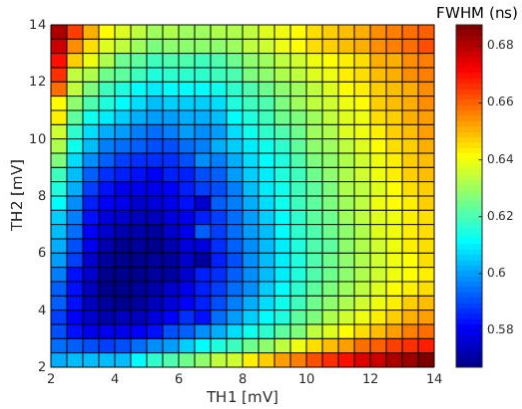
Thus, the single time resolution of the reference PMT is 423 ps (FWHM) and will be used for the all following MPPC measurements.



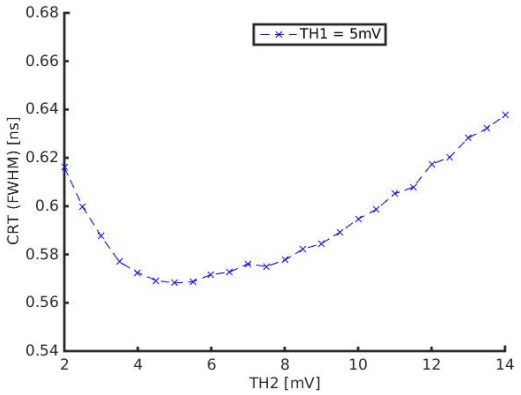
(a) Waveforms of single event



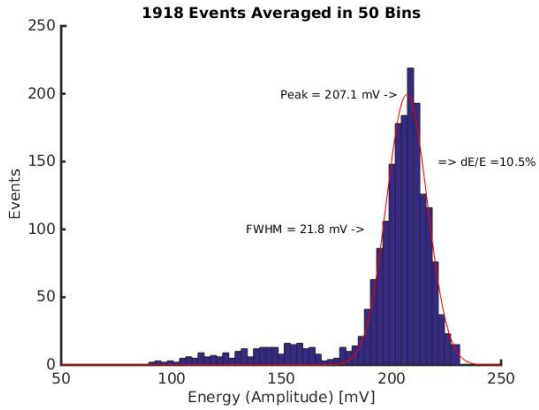
(b) Time resolution histogram



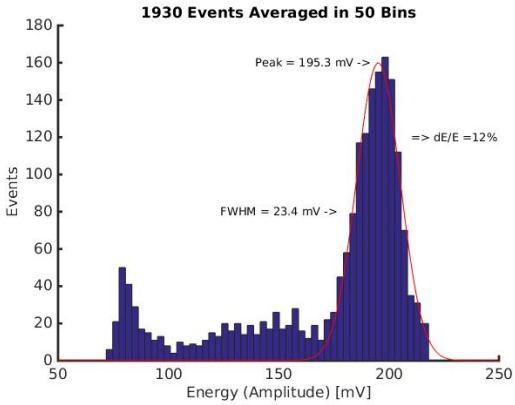
(c) 2D CRT-test



(d) 1D CRT-test

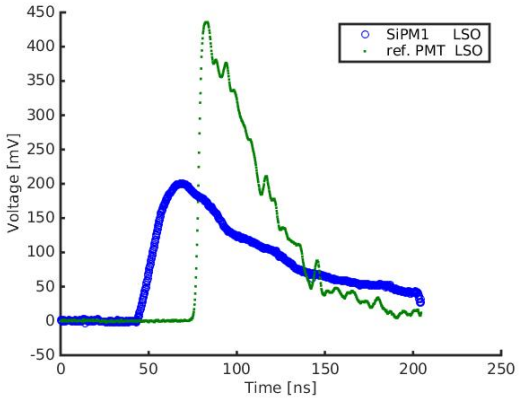


(e) Amplitude distribution for SiPM1

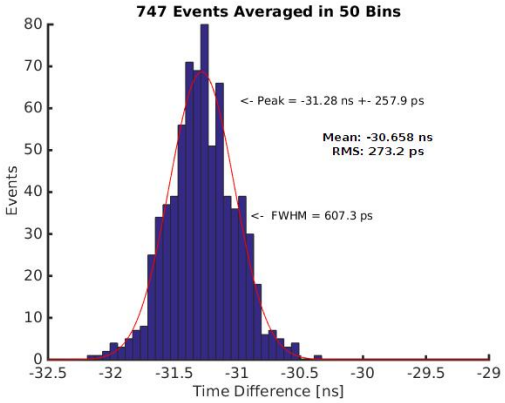


(f) Amplitude distribution for SiPM2

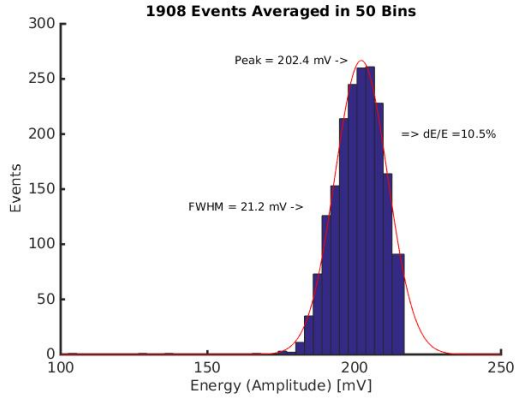
Figure 3.40: CRT-test is shown between SiPM1 and SiPM2. Illustrated in (a) is a coincident PET-event when digitizing at 5 GSPS. (e) and (f) show its dedicated (uncorrected) $\frac{\Delta E}{E}$. (c) and (d) show the CRT-test results for a 2D and a 1D illustration. The histogram in (b) illustrates the best time resolution of 560 ps (FWHM) with TH settings of TH1 = 5 mV and TH2 = 5 mV.



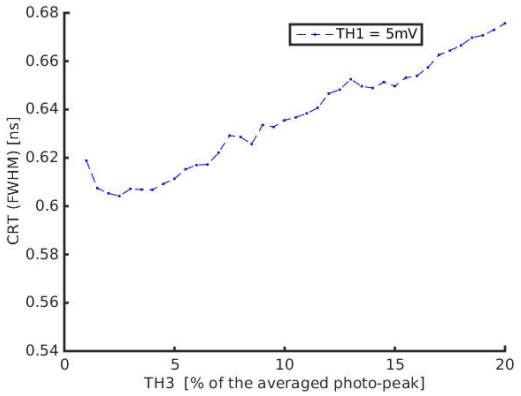
(a) Waveforms of single event



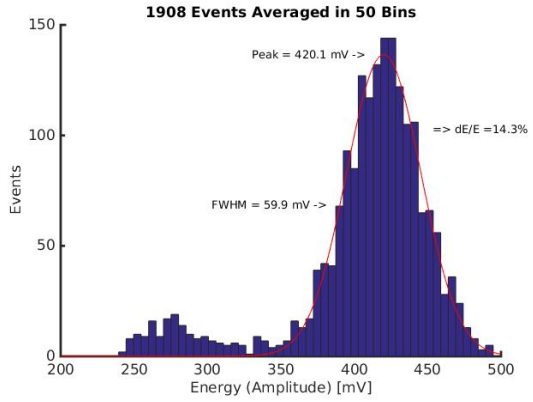
(b) Time resolution histogram



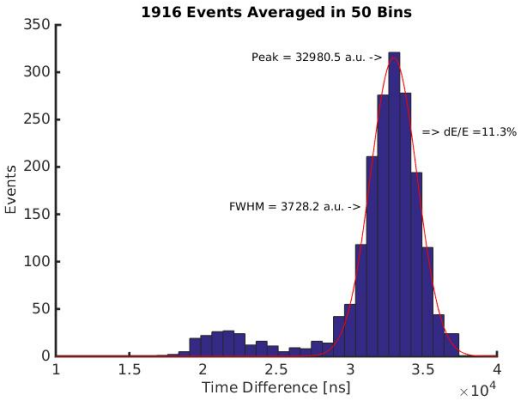
(c) Amplitude distribution for SiPM1



(d) 1D CRT-test

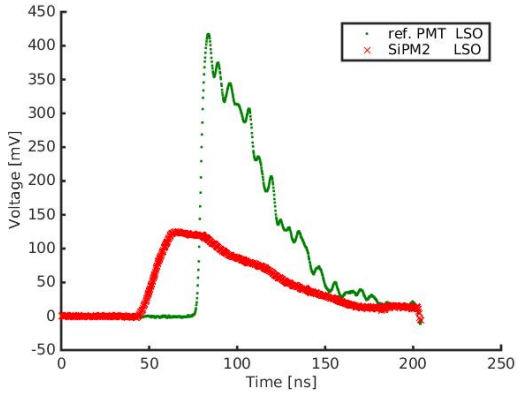


(e) Amplitude distribution of reference PMT

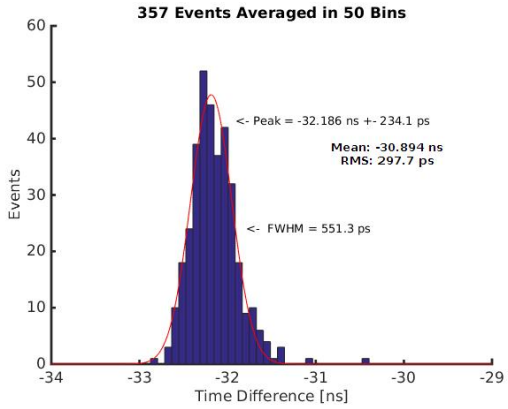


(f) Energy distribution of reference PMT

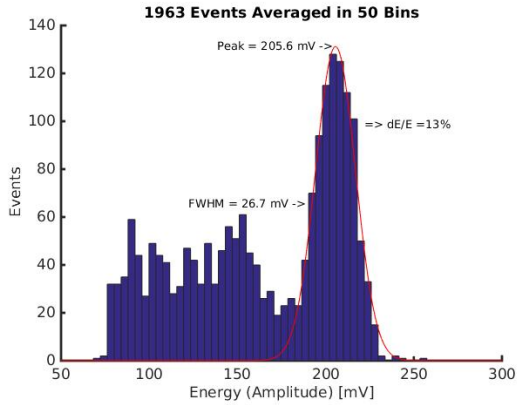
Figure 3.41: CRT-test is shown between SiPM1 and the reference PMT. Illustrated in (a) is a coincident PET-event when digitizing at 5 GSPS. (c),(e) and (f) show its dedicated $\frac{\Delta E}{E}$. (d) shows the time resolution results for different THs. The histogram in (b) illustrates the best time resolution of around 607 ps (FWHM) with TH settings of TH1 = 5 mV and TH3 = 2.5 %.



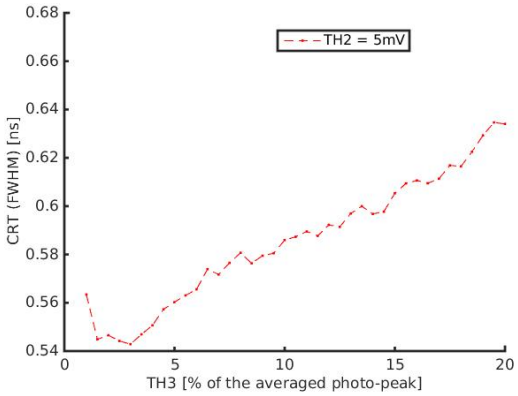
(a) Waveforms of single event



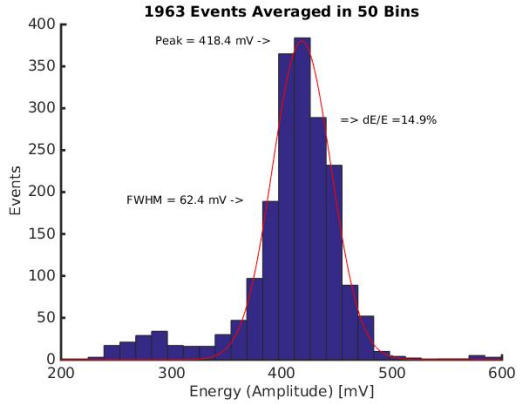
(b) Time resolution histogram



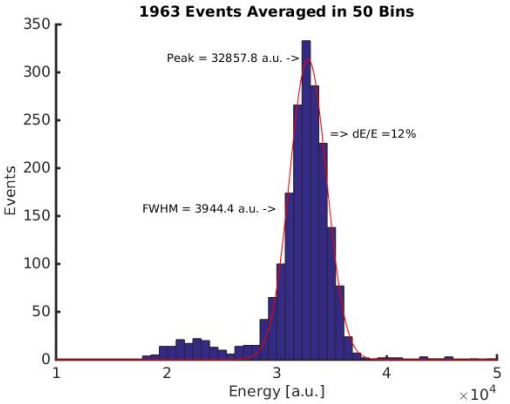
(c) Amplitude distribution for SiPM2



(d) 1D CRT-test



(e) Amplitude distribution of reference PMT



(f) Energy distribution of reference PMT

Figure 3.42: CRT-test is shown between SiPM2 and the reference PMT. Illustrated in (a) is a coincident PET-event when digitizing at 5 GSPS. (c),(e) and (f) show its dedicated $\frac{\Delta E}{E}$. (d) shows the time resolution results for different THs. The histogram in (b) illustrates the best time resolution of around 551 ps (FWHM) with TH settings of TH2 = 5 mV and TH3 = 2.5 %.

3.4.3 CRT-Tests with MPPCs Coupled to PbWO

The CRT-test between the reference PMT and three MPPCs coupled to $PbWO_4$ is shown in this sub-section. More details are available in section 2.5.5. The reference PMT is preset to TH=2.5 % for all three CRT-tests as defined in the previous section 3.4.2. The pitch of the MPPCs, the single photon amplitude and other specifications of the experiment are listed in table 3.10. The utilized amplifier for

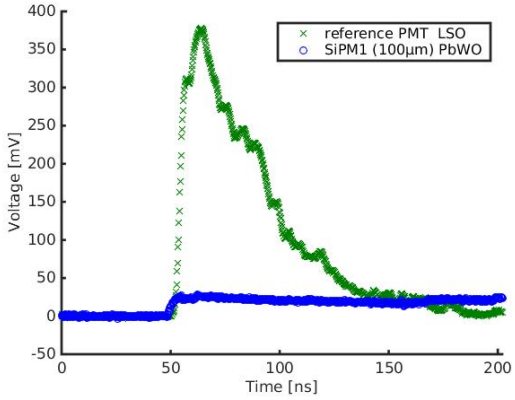
Table 3.10: Listed are the MPPC settings that are used for the $PbWO_4$ experiment. The experiment is held at room temperature using a temperature chamber.

detector	pitch	V_{break}	V_{bias}	PDE	micro cells	single photon
MPPC1	100 μm	70.68 V	71.5 V	≈65 %	100	≈10 mV
MPPC2	50 μm	71.21 V	71.8 V	≈50 %	400	≈8 mV
MPPC3	25 μm	71.19 V	72.0 V	≈25 %	1600	≈37 mV

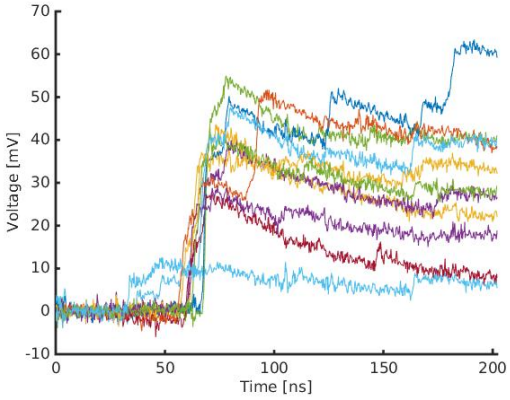
the MPPC is the A1423 Wideband Amplifier from CAEN[107]. It is mandatory to use a trigger logic as described in fig. 2.16 for this experiment. A time window of around 5 ns is used and the trigger TH of the reference PMT is set to 200 mV. The analog trigger TH to capture coincident events is set to approximately 20 mV for MPPC1 and MPPC2. Unfortunately, the analog trigger TH for MPPC3 is set to around 200 mV. The digital LED (2-points interpolation) is chosen for all time measurements . A summary concerning the time resolution of the three CRT-tests is found in table 3.11.

Table 3.11: Listed are the CRT-test results for a PbWO-crystal couped to different MPPCs with a pitch of 100 μm (MPPC1), 50 μm (MPPC2) and 25 μm (MPPC3).

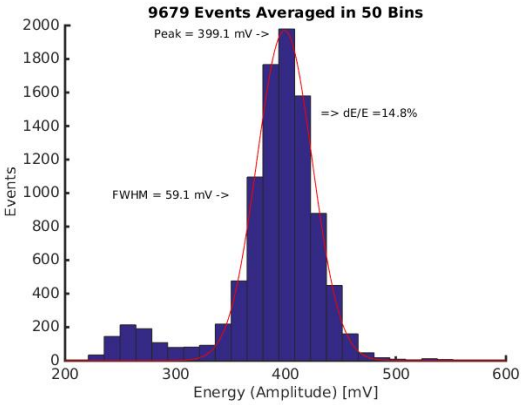
detector	best CRT	best digital LED TH with * condition	details
MPPC1	956 ps (FWHM)	3.5 mV (1^{st} photon) with $>$ 5 photons	fig. 3.43
MPPC2	668 ps (FWHM)	3.0 mV (1^{st} photon) with $>$ 9 photons	fig. 3.44
MPPC3	1162 ps (FWHM)	77 mV (3^{rd} photon) with = 7 photons	fig. 3.45



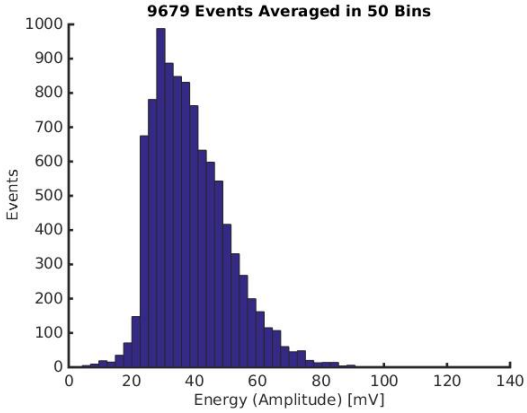
(a) Waveforms of single event



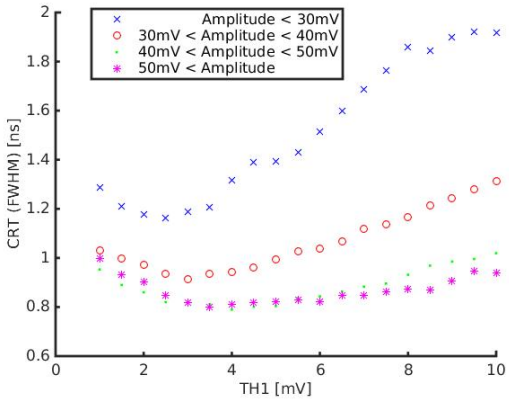
(b) 10 waveforms of MPPC1 channel



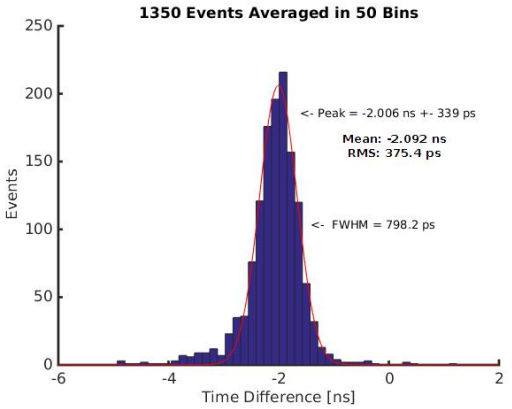
(c) Amplitude distribution of reference PMT



(d) Amplitude distribution for MPPC1

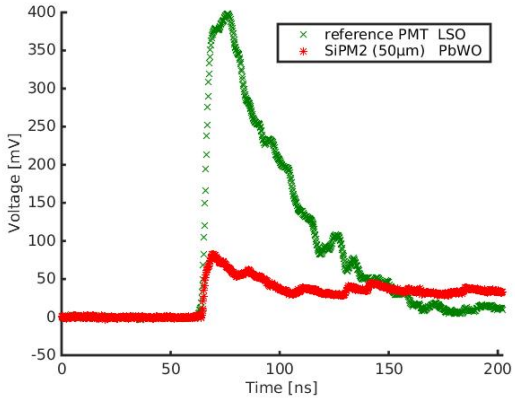


(e) 1D CRT-test

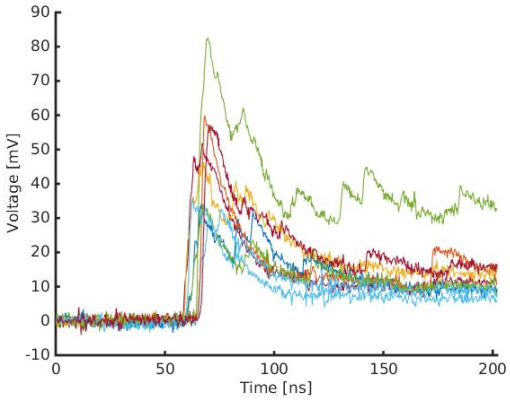


(f) Time resolution histogram

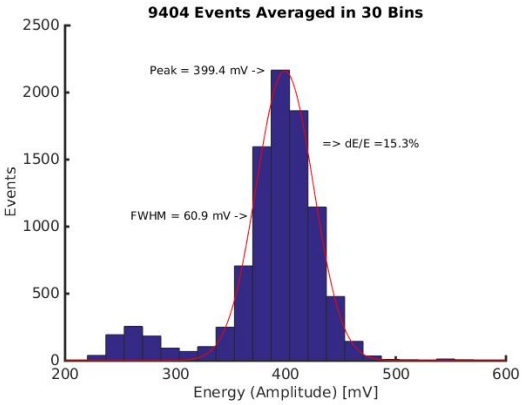
Figure 3.43: Illustrated in (a) is a coincident PET-event when digitizing at 5 GSPS. (b) illustrates some MPPC1 events (100 μm). (c & d) show both amplitude distributions. (e) shows the time resolution results for different THs. The histogram in (f) illustrates the best time resolution of around 798 ps (FWHM) with TH settings of TH1 = 3.5 mV and amplitudes greater than 50 mV.



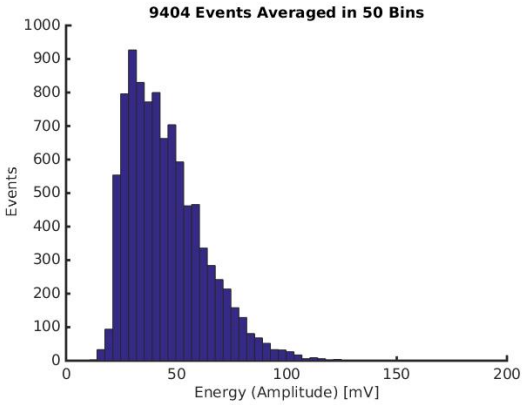
(a) Waveforms of single event



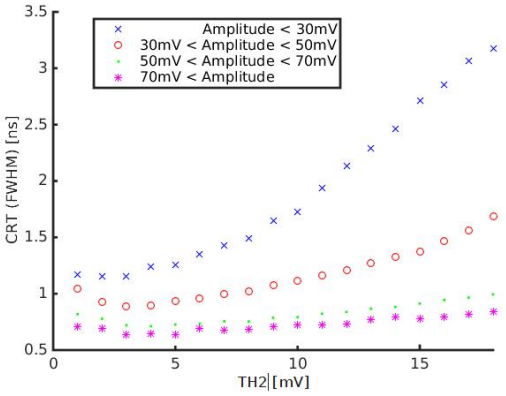
(b) 10 waveforms of MPPC2 channel



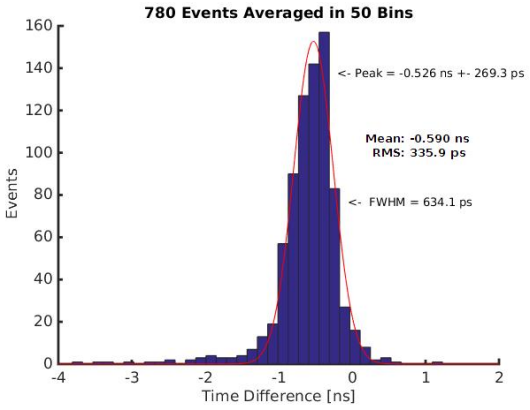
(c) Amplitude distribution of reference PMT



(d) Amplitude distribution for MPPC2

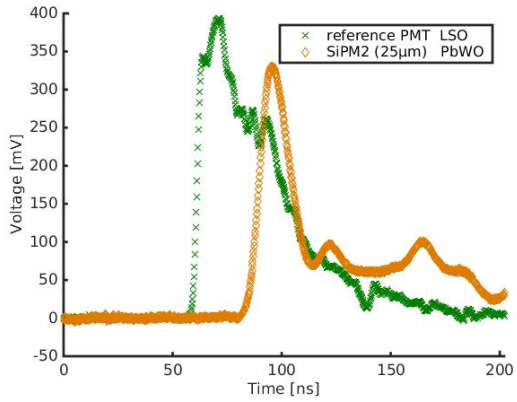


(e) 1D CRT-test

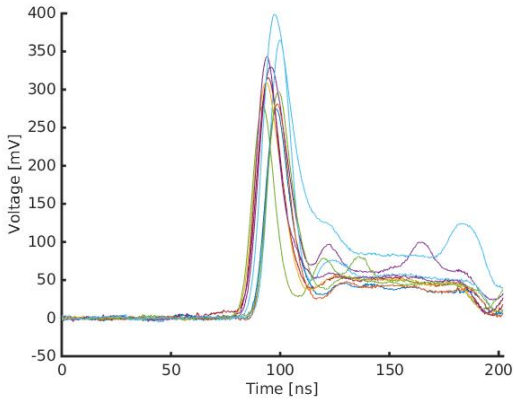


(f) Time resolution histogram

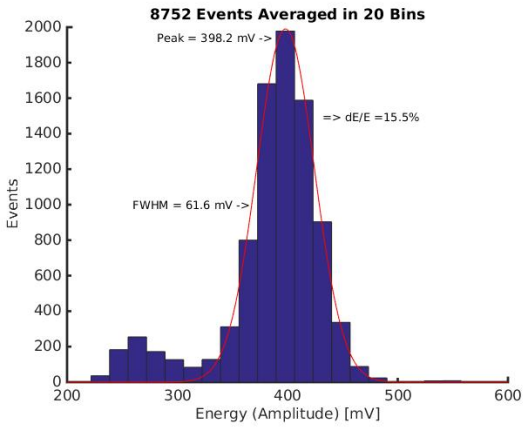
Figure 3.44: Illustrated in (a) is a coincident PET-event when digitizing at 5 GSPS. (b) illustrates some MPPC2 events (50 μm). (c & d) show both amplitude distributions. (e) shows the time resolution results for different THs. The histogram in (f) illustrates the best time resolution of around 634 ps (FWHM) with TH settings of TH2 = 3 mV and amplitudes greater than 70 mV.



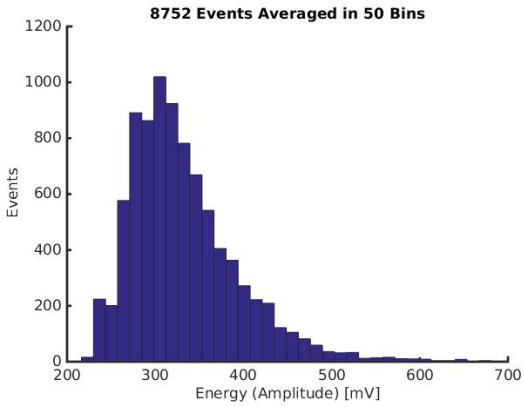
(a) Waveforms of single event



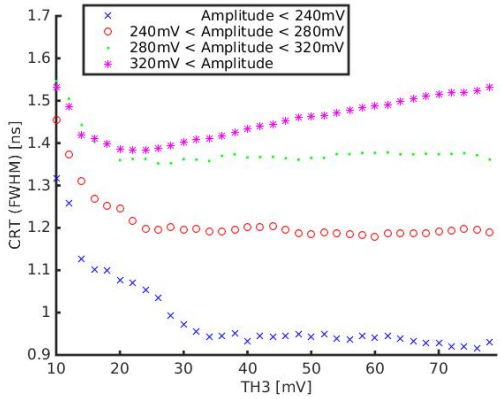
(b) 10 waveforms of MPPC3 channel



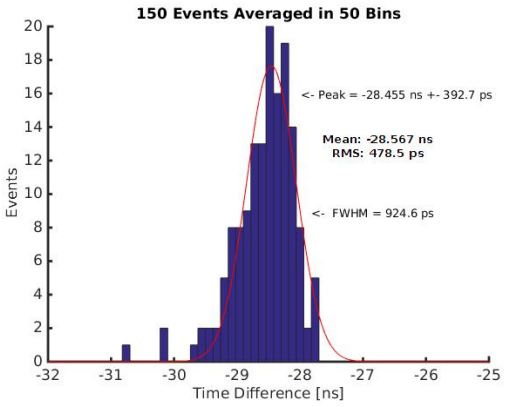
(c) Amplitude distribution of reference PMT



(d) Amplitude distribution for MPPC3



(e) 1D CRT-test



(f) Time resolution histogram

Figure 3.45: Illustrated in (a) is a coincident PET-event when digitizing at 5 GSPS. (b) illustrates some MPPC3 events (25 μm). (c & d) show both amplitude distributions. (e) shows the time resolution results for different THs. The histogram in (f) illustrates the best time resolution of around 925 ps (FWHM) with TH settings of TH3 = 77 mV and amplitudes smaller than 240 mV.

3.5 Other Readout Electronics

Other readout electronics are compared with respect to time resolution in this section and the following 4 sub-sections. The V3 (NEW-TC) results are provided as a reference for most cases. In table 3.12 one will find a summary of all SP-tests for the same cable delay. The cable has approximately a length 10 m resulting in a time delay around 50 ns . If no measurement with a delay of 50 ns is performed for the readout electronics, an approximated time resolution is calculated. Additionally, if no SP-test is performed the result from the P-test is used instead. This rule is applied only if the electronics noise of the P-test is dominant, resulting in an accepted time resolution > 10 ps (σ). This is the case for row 1, 2, 3, 6, 8, 9, 11 and 12. Finally, only measurements are taken into account where a TH of 300 mV is accessible and thus a 2-points digital LED is performed. Additional information which indicate the origin of the listed SP-test values can be found in the entry of column " source " in table 3.12.

3.5.1 V5 from PSI

The V5 was only developed by PSI because of the results of this work. It is therefore also tested with respect to time resolution and sampling frequency[VIII]. Fig. 3.46 shows the NEW-TC outcome of the V5, which means that an external 100 MHz sine wave is applied for the TC-method. The NEW-TC is explained in section 2.2.7. The corresponding V5-TC outcome, where the internal V5 clock is used, looks almost identical and is therefore not shown again.

The V5-TC is only tested for 5.12 GSPS. The SP-test result is shown in row #14 of table 3.12. The P-test is summarized in table 3.13 (row #17 and row #18). The V5-TC also calibrates other sampling speeds[IX] but the performance is not tested. The software update of the V5-board enables the tests directly with histogramming capabilities. Unfortunately, this update is inspired by this thesis and therefore not

[VIII] In section 3.3.3 one can find the SP-test results between the two independently running V3 and V5.

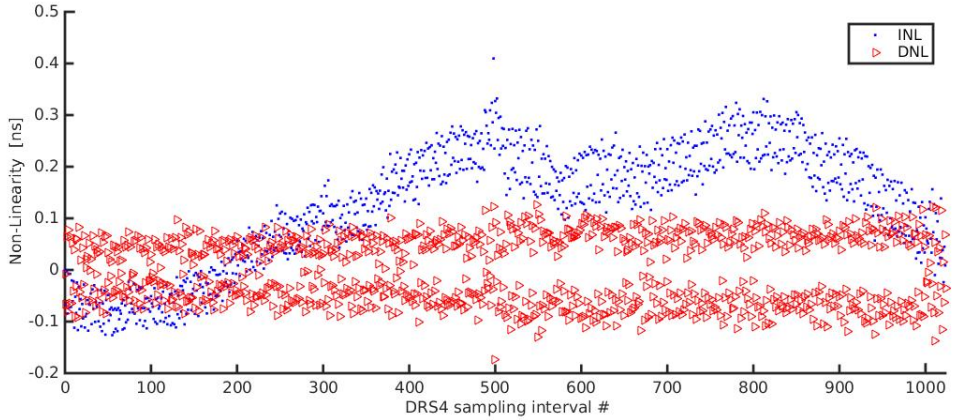
[IX] The V5-TC does not calibrate the sampling speed of 0.7 GSPS. It fails when activated in the V5 software.

Table 3.12: Listed are the SP-tests for all introduced readout electronics with a delay of 50 ns. All DRS4-based boards utilize the original VC provided by their vendors.

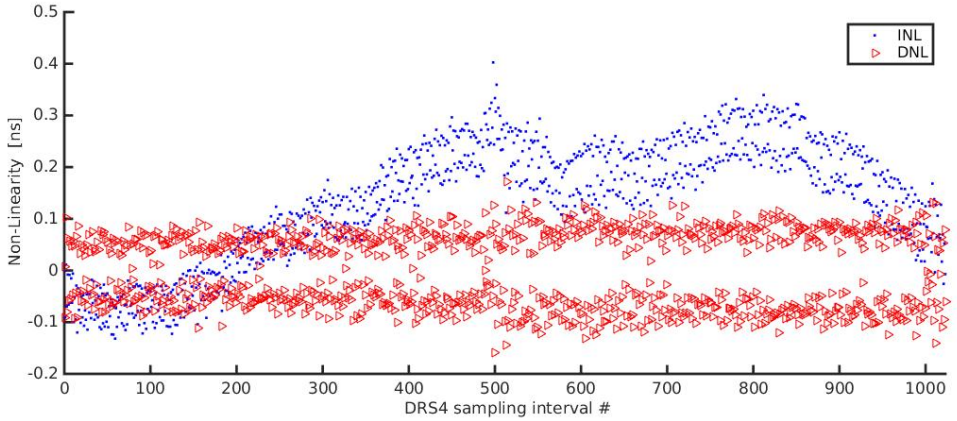
row	readout electronics	settings	source	FWHM	σ
1	V3 (NO-TC)	5.12 GSPS	fig. 3.2(a)	≈1.2 ns	≈0.5 ns
2	V3 (NO-TC)	2 GSPS	fig. 3.2(a)	≈1.4 ns	≈0.6 ns
3	V3 (NO-TC)	1 GSPS	fig. 3.2(a)	≈1.7 ns	≈0.7 ns
4	V3 (V3-TC)	5.12 GSPS	fig. 3.4(a)	≈105 ps	≈45 ps
5	V3 (V3-TC)	2 GSPS	fig. 3.4(a)	≈140 ps	≈60 ps
6	V3 (V3-TC)	1 GSPS	fig. 3.3(a)	≈400 ps	≈170 ps
7	X742 (CAEN-TC)	5 GSPS	fig. 3.21	≈60 ps	≈25 ps
8	X742 (CAEN-TC)	2 GSPS	fig. 3.20(a)	≈105 ps	≈45 ps
9	X742 (CAEN-TC)	1 GSPS	fig. 3.20(a)	≈340 ps	≈144 ps
10	V3 (NEW-TC)	5.12 GSPS	fig. 3.34(a)	≈7 ps	≈3 ps
11	V3 (NEW-TC)	2 GSPS	fig. 3.31(a)	≈24 ps	≈10 ps
12	V3 (NEW-TC)	1 GSPS	fig. 3.32(a)	≈71 ps	≈30 ps
13	X742 (NEW-TC)	5 GSPS	fig. 3.47(d)	≈12 ps	≈5 ps
14	V5 (V5-TC)	5.12 GSPS	section 3.5.1	≈7 ps	≈3 ps
15	V5 (NEW-TC)	5.12 GSPS	section 3.5.1	≈7 ps	≈3 ps
16	V3 & V5 (NEW-TC)	5.12 GSPS	fig. 3.35(c)	≈10 ps	≈4 ps
17	S20 (800 mV range)	20 GSPS	table 3.14	≈30 ps	≈13 ps
18	S5 (1000 mV range)	5 GSPS	fig. 3.47(a)	≈65 ps	≈28 ps
19	NIM-TAC (14bit)	50 ns = 5 V	table 3.15	≈26 ps	≈11 ps
20	NIM-TAC (12bit)	50 ns = 5 V	table 3.15	≈52 ps	≈22 ps
21	NIM-LED	TH = 300 mV	table 3.15	≈9 ps	≈4 ps
22	NIM-CFD	8 cm delay	table 3.15	≈14 ps	≈6 ps

available while working with the V3. However, the update is a key function for quick performance tests or live analyses of experiments.

The baseline noise of the V5-VC shows similar performance compared to the V3-VC. Additionally, the two-state-effect from the V3 illustrated in fig. 3.1 is not measurable anymore. The sampling speed of 5.12 GSPS is tested to be exactly



(a) Channel #2



(b) Channel #4

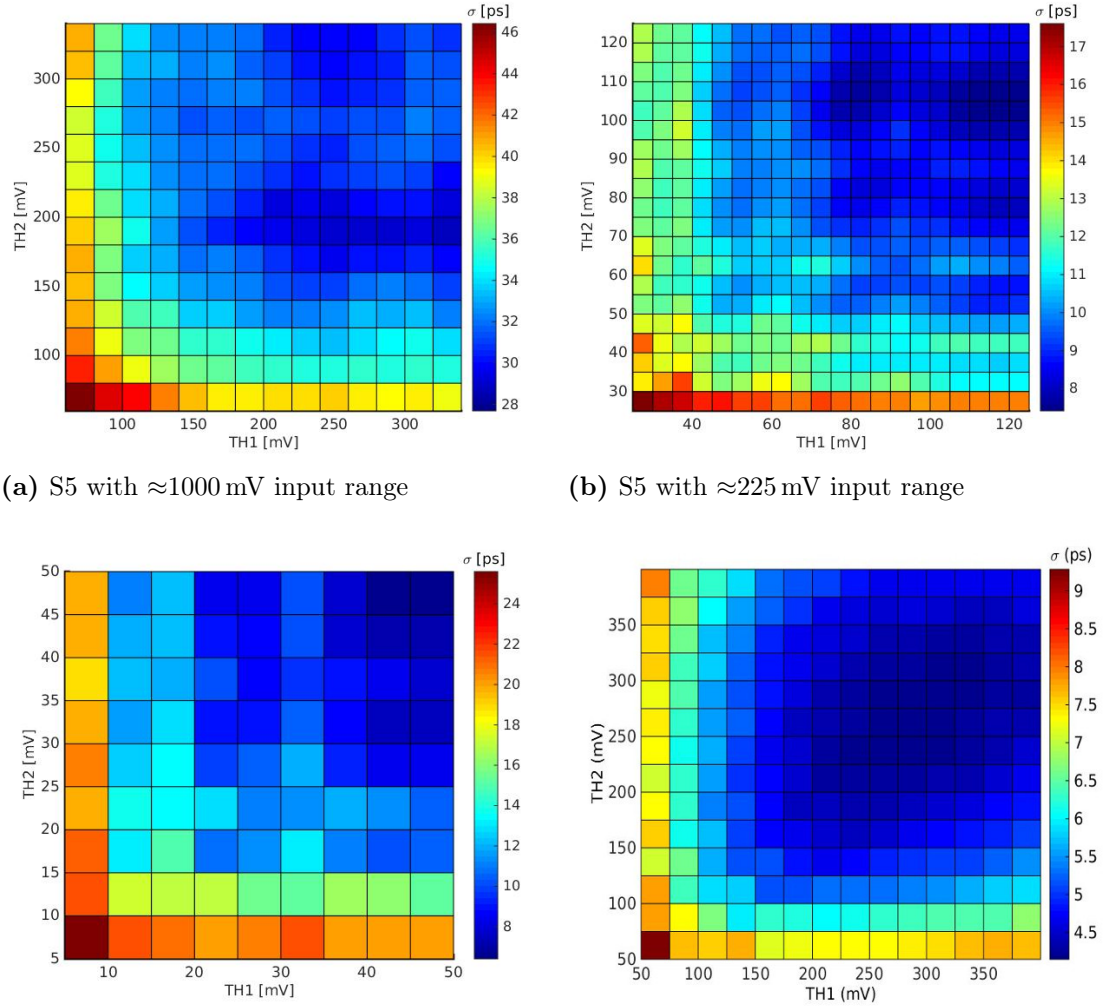
Figure 3.46: In (a) and (b) one will find the INL and the DNL for an ideal-calibrated V5 when running at 5.12 GSPS. Illustrated are two of the four channels.

5.12 GSPS±0.000002 GSPS. Thus, the fluctuation of the V5 is similar to fig. 3.27(a) and no timing improvement compared to the V3 is noted if the correct f_{SCA} is known.

3.5.2 Oscilloscope 6050A (S5)

The reference time resolution tests of the S5 are shown for variating amplification settings of two S5 channels in this sub-section. The digitizers are running at around 5 GSPS for all tests. A more detailed description about the S5 can be found in section 2.4.3.

The 100 MHz P-test (1st period) of the S5 in comparison to the DRS4-chip is illustrated in table 3.13. One can see that different TC-methods (3rd column) are tested



(a) S5 with ≈1000 mV input range

(b) S5 with ≈225 mV input range

(c) S5 with ≈113 mV input range

(d) X742 with ≈1064 mV input range

Figure 3.47: All matrices show the time resolution results for the SP-test (2-points interpolation) using a 50 ns delay and a digitization of 5 GSPS. For (a), (b) and (c) the S5 is utilized with different amplification settings resulting in 27.7 ps, 7.4 ps and 6.4 ps (σ) for ideal TH settings. In (d) one will find the SP-test result for the X742 utilizing the NEW-TC in combination with the CAEN-VC. With optimal TH settings a result of 4.4 ps (σ) is achieved.

for the DRS4-chip. The mean value (6^{th} column) of the period times and its resulting time resolution (7^{th} column) are calculated by a Gaussian fit. Each histogram used for the fit consists of >100k measured periods. The baseline noise (5^{th} column) is measured by applying a DC offset produced by the function generator. Afterwards the function generator settings are switched to compute the periods of the 100 MHz sine wave (1V peak-to-peak). The theoretical time resolution (8^{th} column) is calculated with (1.17). The variables in (1.17) are $A_p \approx 63\,\text{mV}$ and $t_r = 200\,\text{ps}$

Table 3.13: Summarized are the P-tests for the S5 (5 GSPS) and DRS4-based boards (5.12 GSPS) when measuring the first period of a 100 MHz sine wave. All DRS4-based boards utilize the original VC provided by their vendors, except rows labeled with stars. The (*) means that the NEW-VC, the VC3 and the VC5 is utilized. The (**) means that the NO-VC is utilized

row	digitizer	method	range	noise	offset	σ	$\sigma_t \cdot \sqrt{2}$
1	S5 (ch1)	-	≈1000 mV	5.21 mV	-0.01 ps	20.88 ps	23.39 ps
2	S5 (ch2)	-	≈1000 mV	4.42 mV	-0.05 ps	16.72 ps	19.84 ps
3	S5 (ch1)	-	≈225 mV	1.03 mV	0.08 ps	5.17 ps	4.62 ps
4	S5 (ch2)	-	≈225 mV	0.87 mV	0.01 ps	4.64 ps	3.91 ps
5	S5 (ch1)	-	≈113 mV	0.57 mV	0.05 ps	3.92 ps	2.56 ps
6	S5 (ch2)	-	≈113 mV	0.48 mV	0.02 ps	3.62 ps	2.15 ps
7	S5 (ch1)	-	≈56 mV	0.39 mV	0.03 ps	3.54 ps	1.75 ps
8	S5 (ch2)	-	≈56 mV	0.33 mV	0.01 ps	3.36 ps	1.48 ps
9	V3 (ch2)	NO-TC	≈1000 mV	0.41 mV	1.06 ps	≈120 ps	1.84 ps
10	V3 (ch4)	NO-TC	≈1000 mV	0.43 mV	1.49 ps	≈120 ps	1.93 ps
11	V3 (ch2)	V3-TC	≈1000 mV	0.41 mV	4.50 ps	48.05 ps	1.84 ps
12	V3 (ch4)	V3-TC	≈1000 mV	0.43 mV	3.21 ps	52.11 ps	1.93 ps
13	V3 (ch2)	NEW-TC	≈1000 mV	0.41 mV	0.00 ps	3.11 ps	1.84 ps
14	V3 (ch4)	NEW-TC(*)	≈1000 mV	0.43 mV	0.00 ps	3.23 ps	1.93 ps
15	V3 (ch2)	ch4 NEW-TC	≈1000 mV	0.41 mV	-0.06 ps	13.07 ps	1.84 ps
16	V3 (ch4)	ch2 NEW-TC	≈1000 mV	0.43 mV	0.05 ps	13.21 ps	1.93 ps
17	V5 (ch1)	V5-TC	≈1000 mV	0.40 mV	0.00 ps	3.05 ps	1.80 ps
18	V5 (ch1)	NEW-TC(*)	≈1000 mV	0.39 mV	0.00 ps	2.99 ps	1.80 ps
19	X742	CAEN-TC	≈1060 mV	0.45 mV	0.46 ps	23.71 ps	2.02 ps
20	X742	NEW-TC(*)	≈1060 mV	0.38 mV	0.00 ps	2.87 ps	1.71 ps
21	X742	NEW-TC(**)	≈1060 mV	8.56 mV	0.00 ps	51.25 ps	38.43 ps

and result from fig. 2.11(d). The theoretical time resolution is calculated with the provided variables A_p, t_r and the individual noise levels multiplied by $\sqrt{2}$. The $\sqrt{2}$ is mandatory because two linear interpolations have been performed to compute the 1^{st} period times of the 100 MHz sine wave.

The SP-tests of a 50 ns delay for the S5 and the V3[X] are found in fig. 3.47.

The time resolution is 28 ps (σ) when the amplification of the S5 is set to a range where the analog signal is completely visible on the oscilloscope screen (50 mV/division), as illustrated in fig. 3.47(a).

3.5.3 Oscilloscope 640Zi (S20)

The CRT-test with two PMTs (anode) coupled to LSO:Ca (more details in section 2.5.6) is repeated with the S20 in this sub-section. Additionally, an SP-test is utilized to measure the electronics noise of the S20.

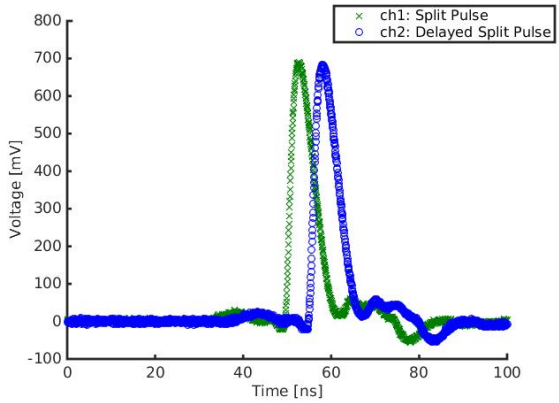
The S20 is the best available readout electronics with the fastest sampling speed in this work. A more detailed description of the S20 can be found in section 2.4.3. The S20 results are found in fig. 3.48 and a summary of these results including the S20 settings in table 3.14. One can see that three measurement results are shown, one SP-test and two CRT-tests. The SP-test is performed with the highest BW of 4 GHz and the fastest sampling speed of 20 GSPS. In both CRT-tests the BW is kept at 1 GHz but the sampling speed is changed from 20 GSPS to 5 GSPS.

Table 3.14: Summarized are the CRT-test and SP-test results and settings of S20. Each row refers to a specific picture of fig. 3.48.

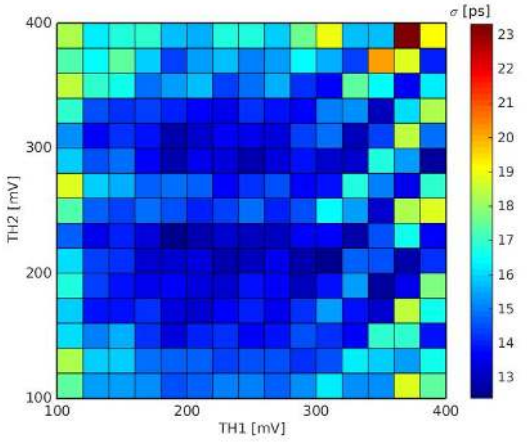
fig.	speed	BW	range	noise ch1	noise ch2	bits ch1	bits ch2
(a)	20 GSPS	4 GHz	≈800 mV	2.81 mV	2.05 mV	≈7.9 bits	≈8.3 bits
(c)	5 GSPS	1 GHz	≈1600 mV	6.51 mV	4.34 mV	≈7.9 bits	≈8.5 bits
(e)	20 GSPS	1 GHz	≈1600 mV	3.97 mV	2.82 mV	≈8.7 bits	≈9.1 bits

fig.	$\frac{\Delta E}{E}$ ch1	$\frac{\Delta E}{E}$ ch2	best TH1	best TH2	delay	FWHM	σ
(b)	-	-	300 mV	200 mV	≈5.4 ns	29.2 ps	12.4 ps
(d)	8.5 %	8.1 %	14 %	16 %	≈2.2 ns	186.4 ps	79.2 ps
(f)	8.5 %	8.0 %	15 %	16 %	≈2.2 ns	180.7 ps	76.7 ps

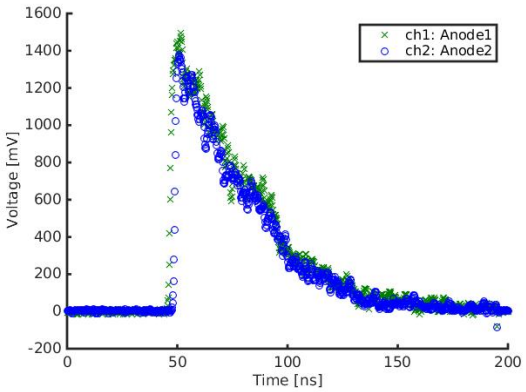
[X] A summary of all SP-test with a delay of 50 ns can be found in table 3.12.



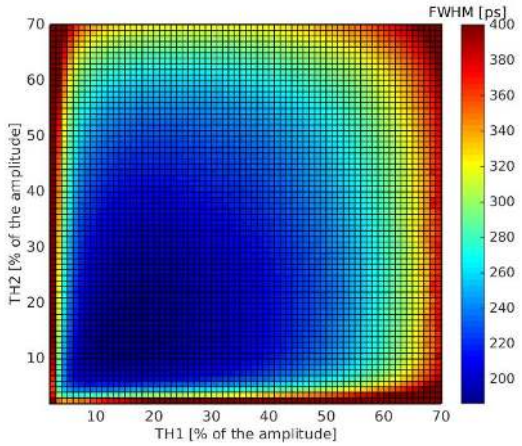
(a) Waveforms SP-test (20 GSPS)



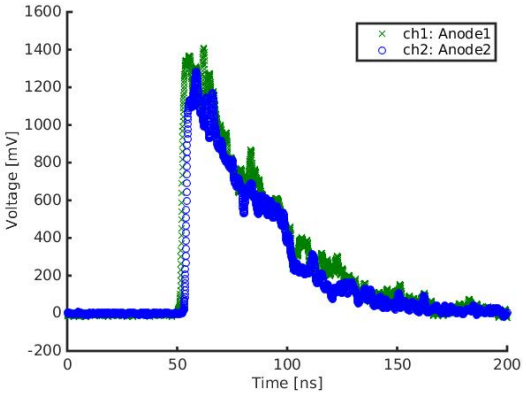
(b) 2D SP-test result (20 GSPS)



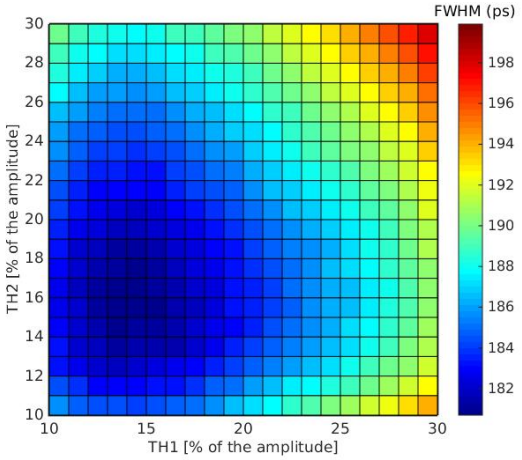
(c) Waveforms CRT-test (5 GSPS)



(d) 2D CRT-test result (5 GSPS)



(e) Waveforms CRT-test (20 GSPS)



(f) 2D CRT-test result (20 GSPS)

Figure 3.48: Illustrated in (a) is an SP-test event. (c) and (e) illustrate example coincident events of a CRT-test. (b),(d), and (f) present the dedicated 2D time resolution results for variating TH settings. The best time resolution settings for the S20 are listed in table 3.14.

3.5.4 NIM Electronics

The SP-test results when utilizing the NIM Electronics are shown in comparison to the V3 (NEW-TC) in this sub-section. More details about the tested components are provided in section 2.4.4. The experimental test setup of the NIM-TAC module is identical as sketched in fig. 1.8, but with the difference that the two PMT channels have been replaced with a split pulse. The NIM-TAC is preset to a time range of 50 ns resulting in 5 V for 50 ns and 0 V for 0 ns measured delays. The voltages from 0 V to 5 V have been measured with two ADC solutions, 12 bit and 14 bit. The two delay cables utilized for the NIM-TAC are measured to be exactly 4 m. The cable for the V3 (NEW-TC) measurements is approximately 10 m long. The THs for the two utilized NIM-LED, NIM-CFD and V3 channels have been set to 300 mV, consistent with the other SP-tests. The results of the tested NIM modules are listed in table 3.15.

Table 3.15: Summarized are the SP-tests of all introduced NIM modules in comparison with the V3.

row	NIM electronics test combination	delay 1	delay 2	σ (delay 1)	σ (delay 2)
1	NIM-LED + NIM-TAC + 12 bit ADC	≈20 ns	≈40 ns	21.7 ps	21.8 ps
2	NIM-LED + NIM-TAC + 14 bit ADC	≈20 ns	≈40 ns	10.3 ps	10.9 ps
3	NIM-CFD + NIM-TAC + 14 bit ADC	≈20 ns	≈40 ns	10.4 ps	11.1 ps
4	NIM-LED + V3 (NEW-TC)	≈50 ns	-	5.1 ps	-
5	NIM-CFD + V3 (NEW-TC)	≈50 ns	-	6.8 ps	-
6	V3 (NEW-TC)	≈50 ns	-	3.2 ps	-

Chapter 4

Discussion

The fastest sampling technology, the flash ADC, has reached a point where cost per channel, power consumption and timing performance are limited. Therefore, several SCA-chips have been developed by individual vendors like the SAM-chip[69], the LABRADOR-chip[70], the PSEC4-chip[71], the DRS4-chip[68], etc. The DRS4-chip[I] which is exclusively investigated in this work, is implemented in several research fields like particle physics (e.g. the MEG experiment [72]), neutrino physics (e.g. the ANTARES experiment [75]) or astronomy (e.g. the MAGIC telescope [73]) to name a few. Even if the same SCA-chip is utilized each research group develops its own dedicated SCA-calibrations and specialized timing algorithms. Thus, the measured timing of an SCA-chip depends on the applied calibrations and the timing algorithms as visible in table 4.1. One can see in row #1 of table 4.1 that the DRS4 time resolution of the original calibration from PSI (V3-TC[II]) was expected to be around 25 ps (σ) due to Adam et al[72]. Row #3 confirms this assumption for the V3-TC but only if multiple points of the waveform are utilized for the timing calculation. If on the other hand only 2 points of the rising edge are used (row #2), the time resolution of the DRS4-chip lies around 27-52 ps. Utilizing the same algorithm, the CAEN-TC provides improved results for the DRS4-chip with a time resolution between 19−30 ps (row #5). The publication from Wang et al[96] where the DRS4-chip is differently

[I]The DRS4-chip was designed in the year 2007. Its oldest parent, the *Domino Sampling Chip* (DSC), was designed in 1998[108].

[II]The original time calibration method for the Domino Ring Sampler series (DRS2, DRS3 & DRS4) is referred to as "V3-TC" in this work because this TC is provided together with the V3. Starting with the V5 the NEW-TC is utilized.

Table 4.1: Listed are the best timing results of 3 SCA-chips when utilizing different calibration methods and timing algorithms. The numbers are taken from SP-test-figures or publications and are listed in the column "source". The rows labeled with * utilize TC-methods which are not introduced nor tested in this work. More details about these TC-methods are written in this chapter and origin from the provided references.

row	SCA	TC-method	timing	algorithm	dependence	source
1	DRS4	V3-TC	ca. 25 ps	?	?	Adam[72]
2	DRS4	V3-TC	27-52 ps	2-SPs LED	random	fig. 3.4(a)
3	DRS4	V3-TC	15−35 ps	50-SPs PCC	periodic	fig. 3.4(b)
4	DRS4	V3-TC	ca. 5 ps	50-SPs PCC	0−1 ns	fig. 3.4(b)
5	DRS4	CAEN-TC	19−30 ps	2-SPs LED	random	fig. 3.21
6	DRS4	CAEN-TC	ca. 8 ps	2-SPs LED	0−1 ns	fig. 3.21
7	DRS4	CAEN-TC	8−18 ps	50-SPs PCC	periodic	fig. 3.21
8	DRS4	CAEN-TC	ca. 4 ps	50-SPs PCC	0−1 ns	fig. 3.21
9	DRS4	LTC*[96]	ca. 9 ps	10-SPs CFD	4 ns delay	Wang[96]
10	DRS4	NEW-TC	2.3−3.3 ps	2-SPs LED	0−60 ns	fig. 3.34(a)
11	DRS4	NEW-TC	0.8−2 ps	50-SPs ICC	0−60 ns	fig. 3.34(a)
12	PSEC4	zeros*[71]	4−9 ps	20-SPs fit	0−20 ns	Oberla[71]
13	SAMPIC	LTC*[74]	4−6 ps	2-SPs CFD	random	Breton[109]
14	SAMPIC	LTC*[74]	ca. 3 ps	2-SPs CFD	0−1 ns	Breton[109]
15	SAMPIC	LTC*[74]	3−5 ps	20-SPs CC	random	Breton[109]
16	SAMPIC	LTC*[74]	ca. 2 ps	20-SPs CC	0−1 ns	Breton[109]

calibrated with a costly LTC method, shows performance results around 9 ps (RMS) for optimized analog signal conditions and a multi-points timing algorithm (row #9). This DRS4-result is an improvement compared to V3-TC but equivalent to the CAEN-TC when utilizing multiple points of an ideal signal with a delay of 4 ns (row #9 vs. row #7). To date, the second best reported time resolution among SCA-chips under optimized conditions lies around 4 ps (row #12 and row #15). The PSEC4-chip is calibrated by counting zero-crossings of a periodic signal[71]. Its time resolution when utilizing more than 20 points for the timing algorithm, lies between 4−9 ps linear increasing with the delay (row #12). The extravagant LTC-

solution[74] of the SAMPIC-chip achieves around 5 ps for a 2-points method and only around 4 ps for a CC-solution although using 10 times more points (row #13 vs. row #15). Like the V3-TC and the CAEN-TC, also the SAMPIC-chip shows disproportionately good results for delays smaller 1 ns which indicates a non-ideal calibration (row #4, row #6, row #8, row #14 and row #16). Additionally, for all three calibrations the time resolution vs. the delay randomly/periodically fluctuates and thus underlines that an inferior TC-method is used. The publication in the year 2014[31] where a fraction of this work has already been published, introduces the best ever measured time resolution for an SCA-chip. A time resolution below one picosecond was accomplished if the correct TC-method is applied. Demonstrated in this thesis is the associated histogram of this publication which shows a time resolution of 820 *Femtoseconds* (fs) for the DRS4 when utilizing an easily applicable cross-correlation method (row #11 and fig. 1.4 showing the 50-points ICC histogram). Moreover, when using two points instead of 50 points already results in a time resolution below 3 ps for the DRS4-chip with the correct calibration (row #10).

In the next lines the discussion chapter continuous regarding other DRS4-results in which the following 11 sections continuously will be referred to for deeper discussions. As stated before, the key to enable the full potential of the SCA-technology is accurate calibrations (VC and TC). Improving these calibrations is a major topic of this work and is investigated for two realizations of DRS4-based boards, from PSI and from CAEN (detailed hardware comparison in section 4.1). The VC is well understood by PSI but there is still potential for the DRS4-based boards from CAEN (more details in section 4.2). The investigated CAEN-TC is approximately twice as effective as the V3-TC from PSI. CAEN partially adopted and improved the V3-TC around 2011, when CAEN announced their first DRS4-based board with 32 channels. "Adopted" because the Δt_b behavior looks identical to the V3-TC with $\Delta\bar{t}_b = 200\pm3$ ps for an f_{SCA} of 5 GSPS. And "Improved" because the time resolution looks better compared to the V3-TC as summarized in table 3.12 (row #4 vs. row #7). The improvement is caused by the better TC-signal which is used for the CAEN-TC (more details in section 4.3). Still, the CAEN-TC and the V3-TC are approximately one order of magnitude away from the achievable time resolution as

it is demonstrated in this thesis.

At the very beginning of the work with the DRS4, pre-clinical PET-measurements (CRT-test) were performed satisfactorily with SiPMs (see section 4.9) and APDs (see section 4.8), because its results showed the expected time resolutions and Gaussian distributions for CRTs greater than 500 ps (FWHM). In contrast, a better CRT than theoretically expected was discovered for CRT-tests crossing the 300 ps border (details in section 4.10). Problems were also discovered for artificial signals (P-test and SP-test) as they are described in the first two sections of chapter 3 in which the DRS4-chip is tested with the original TCs from PSI and CAEN. Summarized, the four first discovered problems are the unpredictable time resolution function vs. the cable delay, a non-Gaussian distribution behavior, worse time resolution than expected (details in section 4.3) and simultaneously better time resolution than expected for some CRT-tests. In June 2012 the NEW-TC development started investigating these problems.

The first successfully working TC for the DRS4-chip is developed in this thesis. It utilizes more than 40 frequencies and is called the FTC. The FTC is a reliable TC-method of the NEW-TCs, because it uses the most uncorrelated statistics (more details in section 4.3). The FTC solved all problems that resulted from the usage of previous TC-methods for the DRS4-chip.

By applying the FTC to different DRS4-chips it was identified that the sampling intervals (Δt_b) alternate between two sets of Δt_b as 270 ps, 130 ps, 270 ps, $\cdots$, with a fluctuation of around 20 ps at 5 GSPS (see table 3.9). Note, that the previous TCs predicted an equidistant set of Δt_b as 200$\pm$3 ps. This means that the expected f_{SCA} of 5 GSPS is in reality continuously changing between $\approx$4 GSPS and $\approx$8 GSPS. The reason for this alternating behavior results from the layout of the DRS4-chip. The 1024 sampling cells of an individual channel are not linearly arranged. Instead they are folded due to the limited size of the die. The folding causes a different environment for odd and even cells. A reduced alternating behavior of the DRS4-chip is found at lower sampling speeds. One will also measure a degradation of the time resolution as summarized in table 3.12 (see section 4.4 for more details).

The FTC is approximately 3 times better than the original TC from PSI, when

applied globally to all channels. Also demonstrated in this thesis is an additional timing improvement by a factor of 5 if each channel is calibrated individually. Overall the FTC enabled an timing improvement by a factor of around 15 compared to the V3-TC from PSI as illustrated in fig. 4.1. Additionally, the theoretical time

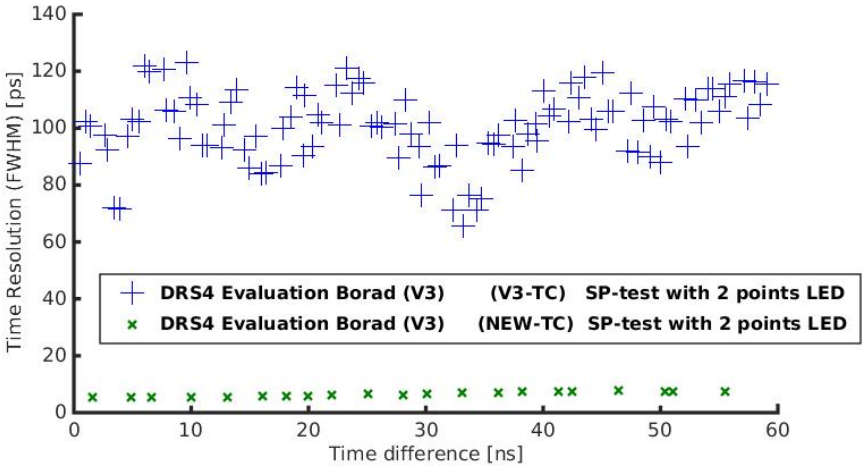


Figure 4.1: The SP-test for the NEW-TC improves approximately by a factor of 15 compared to the original calibration (V3-TC). The DRS4 was sampling with 5.12 GHz and a simple 2-points digital LED is applied in all cases. This figure is created by combining the two curves, fig. 3.34(a) and fig. 3.4(a)

resolution region for given pulses is finally reproduced (see discussion in section 4.6). Although the FTC provides the correct TC, it is too complicated and expensive for a reliable application. Therefore, an easier method was needed to perform a satisfactory TC. This led to the fully evaluated theory for an easier TC-method using only a single waveform. A C-code has been developed which was able to perform this TC-method for any common SCA-chip from individual vendors, including DRS4-based boards. It consists of two parts. The first part (LTC) roughly computes time distances between two neighboring cells. The second part (GTC) corrects afterwards the resulting dataset for time differences between cells that are far apart. These NEW-TCs including the other tested TC-methods from PSI and CAEN are discussed in the following section 4.3

The original TC-method from CAEN (CAEN-TC) provides wrong time resolution results. This would not be so much of a problem if the time resolution performance is simply inferior. Instead some measurements will result in overestimating the time resolution (see section 4.10 for detailed discussion). PSI on the other hand, directly

adopted one of the NEW-TCs and designed a new DRS4-based board, the V5 (more details in section 4.1). The V5 offers almost the full performance of the DRS4. Its performance lies in the sub-picosecond region with regards to time resolution (see discussion in section 4.7).

More details about the DRS4 performance (section 4.1 − section 4.4), its comparison to other readout electronics (section 4.5) and the outcome of the three performance tests, the P-test (section 4.6) the SP-test (section 4.7) and the PET related CRT-test (section 4.8 − section 4.11) is available in the following sections.

4.1 DRS4-Based Boards Hardware Comparison

The results of all investigated DRS4-based boards, comprising the boards from PSI (V3 & V5) and the X742 series from CAEN (DT5742 & V1742), will be discussed in this section.

The X742 enables all channel offsets to be set individually within a range of $\pm 1\,\mathrm{V}$ in mV increments. This is an advantage compared to the V3 or the V5 where the offsets of all channels are adjustable globally between two possibilities ($-0.5\,\mathrm{V}$ & $0\,\mathrm{V}$). However, all boards show the same crosstalk behavior for the utilized DRS4-chip. A signal applied to channel n results in the highest crosstalk value in channel $n+1$ and remains measurable in the following channels ($n+2$, $n+3$, $\cdots$). The lower channel numbers like channel $n-1$ result in a suppressed crosstalk statistics which decreases if located further away from channel n. Thus, if not all DRS4 channels are needed one should not place them next to each other. A low DRS4 channel number is especially recommended for a good time resolution. Thus, for PET applications one should ideally separate timing channels as far left as possible from the energy channels to prevent crosstalk. A crosstalk example is given in fig. 3.18(c & d) where an oscillating signal is applied to the 4^{th} (channel #18) of the nine available DRS4 channels. One can see that in the surrounding channels of channel #18 the baseline noise increases. This is especially the case for the channel #19. Channel #16 has the lowest crosstalk behavior because it is the first channel in this utilized DRS4-chip. Thus, if a channel is chosen for the spike correction (VC3) it should ideally be the

first channel of the DRS4-chip. Unfortunately, this is not the case for the boards from PSI (e.g. the V3 board) where the ninth channel is chosen instead for the VC3. This explains the occasional VC3-failures when a signal is applied to channel #4 of V3 which in fact is the eighth channel of the DRS4-chip. In contrast, VC3-failures in the X742 are much greater. VC3 is included in the CAEN-VC and fails with a relativity high probability as shown in fig. 3.18(b). The high amount of VC3-failures is represented by the increased RMS-noise[III] of all involved DRS4-channels. This is caused by the fact that the CAEN-VC only applies the VC3 if a spike is globally detected in all channels of the DRS4. Since spikes are not detectable anymore if located inside steep edges, the oscillating signal in fig. 3.18(b) will cause a high VC3-failure rate.

Fast oscillating signals with steep edges can also be applied to synchronize multiple DRS4-chips as shown in fig. 3.33. One should consequently share all ninth channels of the DRS4-chips for the synchronization to minimize the before mentioned crosstalk as it is provided in the X742. This so-called "fast trigger" of the X742 is also the only triggerable channel. Additionally, all DRS4-based boards are equipped with a global trigger. The maximum acquisition rate of the PSI boards (V3 & V5) lies around 500/s when all 4 channels are acquired. This acquisition rate is comparable to standard oscilloscopes with 4 channels, like the investigated S5 or the S20 (discussed in section 4.5). The maximum acquisition rate for the X742 increases compared to the V3 by a factor of three combined with a doubling of the digitized channels (8 channels). This is caused by two factors. First, a 50 % faster running multichannel ADC from CAEN where each DRS4-channel gets an exclusive ADC-channel. Second, the USB2.0 cable is only used for the data transfer in the X742 case, whereas in the V3 case the power must be provided additionally. If the USB2.0 cable is replaced with the Optical Fiber cable one can further increase the maximum acquisition rate to around 6000/s (8 channels). However, the global trigger of the X742 has a delay of 260 ns, which makes it useless for an f_{SCA} of 5 GSPS

[III]The RMS value is used instead of the typical Gaussian fit in fig. 3.18(b) to identify the VC3-failures. Therefore, one is more sensitive to outliers and thus one can see that the CAEN spike correction fails permanently. The symmetrical spike problem (VC3) is described in section 2.3.3 and the VC3 algorithm from CAEN is described in section 2.3.7.

(T_{SCA}= 200 ns). Thus, only the fast trigger (delay around 30 ns) can be used for the X742 which limits the amount of usable channels to 16 for the highest sampling speed of 5 GSPS. For the other two sampling speeds of the X742 (1 GSPS & 2 GSPS) all 32 channels can be used in parallel.

The V3 can trigger on a single channel of the four channels (only channel #1) or on the before mentioned global trigger. The V5, which is an improved version of the V3, offers an adjustable trigger logic that includes all four channels. Also the time resolution improves from around 45 ps for the V3 to 3 ps for the V5 (row #4 vs. row #14 in table 3.12). This improvement resulted by replacing the previous TC-method and its dedicated TC-signal. Thus, a time resolution of 3 ps can be achieved with the V3 if the correct TC tables are applied (row #10 in table 3.12). This is also the case for the X742 where the original time resolution is around 25 ps (row #7 vs. row #13 in table 3.12). Further, the measured T_{SCA} of the V3 differs from the expected value by more than 20 ps (>0.01 %) as illustrated in table 3.6. Although, this V3 error does not sound large, correct delays cannot be measured because it is a systematic error. Thus, the measured delay with the V3 (V3-TC) will be longer than expected. One example is demonstrated in fig. 3.27(a & b) where this delay error is reproduced. This is especially problematic for accurate frequency measurements or physics experiments where high precision is required. The X742 does not show the mentioned delay error and runs at the expected f_{SCA}. This is accomplished by a more expensive clock which is also temperature stabilized.

Based on the V3-results in this work, the original clock which regulates the f_{SCA} was replaced for the V5 to guarantee the expected f_{SCA}. The V5-board finally runs at the correct f_{SCA} which is compared to the measured f_{SCA} of the V3 an offset of 0.013 %. This replacement was not necessary, because the true f_{SCA} becomes available with the NEW-TC. It was found for the V3, apart from the f_{SCA} offset of 0.013 %, that the measured f_{SCA} remains constant over a wide temperature range as shown in fig. 3.29. Thus, the V3 provides the same performance as the V5 if the two-state-effect is controlled. The drawback in this case is that one channel is needed as a reference channel and effectively only three channels are left for measurements. If a time resolution of around 5 ps is acceptable (see fig. 3.29(a & b) for details) all four

channels can be used for the V3 under the condition that the NEW-TC is applied together with an external TC-signal. Thus, all older versions of the DRS4 Evaluation Board (e.g. V3) can be upgraded when following the description in section 2.2.9. The results in fig. 3.24(c & d) prove that its internal 66 MHz clock[IV] can be utilized as an external TC-signal.

Compared to the just mentioned upgrade, a more expensive upgrade was made on the V5. In the V5 a third clock consisting of a 100 MHz sine wave with a low time jitter has been integrated. The clock provides the TC-signal which is required for the V5-TC. The V5-TC is a modification of one possible NEW-TC combination extracted from this thesis. The mentioned 100 MHz of the V5 is not the optimal f_{TC} for all sampling speeds but it results in a decent TC-outcome for an f_{SCA} of 5 GSPS. The V5-TC results in a similar SP-test outcome compared to the NEW-TC as shown in table 3.12 (row #14 vs. row #10). The optimal f_{TC} is available when utilizing (2.26). In contrast, the provided f_{TC} of 240 MHz from the V3, which was originally utilized for the V3-TC, has a time jitter greater than 100 ps. This is the main reason why the CAEN-TC looks superior compared to the V3-TC although a similar principle is used to calibrate the boards from PSI or CAEN. Notice that the old principle (V3-TC or CAEN-TC) is inferior to the full performance of the DRS4 which becomes available by a correctly applied NEW-TC.

When taking a closer look at the provided VC-methods, the V3 and therefore the V5 work satisfactorily. In contrast, the X742 offers a lot of potential for improvement in this respect (e.g. the previously mentioned VC3-problem). Fig. 3.18(a) proves that the baseline offset has little fluctuation when histogramming all SPs of 1000 waveforms together, because the resulting baseline offset is around 0.5 mV (σ), regardless of the VC-method. The baseline offset also has a maximum spread of 10 mV as shown in fig. 3.19(a). If the correct VC-methods combined with the NEW-TC are applied to the X742, a superior performance is achieved compared to the V5 as shown in table 3.13 (row #18 vs. row #20). A deeper VC-discussion concerning all DRS4-based boards is provided in section 4.2.

[IV] It is found in this work that the clock frequency is in fact 66.002 MHz for the V3. However, one will find the true clock frequency when calibrating as shown in fig. 3.24(d)

To date all physics experiments that utilize multiple DRS4-chips including the X742 invested a lot of effort in synchronizing the DRS4-chips. The three main hardware simplification achievements of this work are: First, that DRS4-chips do not have to be synchronized to each other. Second, they do not need a global f_{SCA} as long as a reference clock is digitized in one of the nine channels (see section 4.7). The reference clock can also be used as the TC-signal. And third, the clock-temperature that drives the DRS4 is less important compared to the DRS4-temperature. If the DRS4-temperature does not differ more than $\pm 5\,^{\circ}\mathrm{C}$ from the calibration temperature and a 5 ps time resolution is sufficient, the NEW-TC must be applied only a single time and stays valid for more than 3 years as tested in this thesis. A deeper discussion that addresses all investigated and developed TC-methods is provided in section 4.3. All provided numbers in this section relate to an f_{SCA} of 5 GSPS. The other sampling speeds are discussed in section 4.4.

4.2 DRS4 Comparison of all VC-Methods

The NEW-VC which is developed in this thesis provides the VC1 and the VC2 in one step. The NEW-VC shows no measurable improvement compared to the V3-VC from PSI when utilized to the V3 as illustrated in table 3.13(row #12 vs. row #14). This is because both methods are applied to channel #4. A degradation is expected for channel #1, because the VC2 is only needed for channel #1. Since channel #1 is used for the two-state-effect information, no analog signal can be applied and is therefore unavailable for measurements when utilizing the V3. Because of this work PSI was able to solve the two-state-effect challenge, which is realized in the V5 board. Therefore, channel #1 of the V5 is available for a comparison between the NEW-VC and the V3-VC (the V3-VC is identical to the V5-VC). The NEW-VC shows a slightly (0.01 mV) better performance as illustrated in row #17 and row #18 of table 3.13. Summarized, the V3-VC, the V5-VC and the NEW-VC result in a reliable VC1 and VC2 with a typical baseline noise of around 0.37 mV (σ). The mentioned 0.37 mV (σ) are only achievable if no external cables are connected to the PSI boards.

In contrast, the CAEN-VC applied to the V1742 results in a baseline noise greater than 1 mV (RMS) as shown in fig. 3.17(a). Additionally, one can also estimate with fig. 3.17(b) that the baseline noise of 500 SPs (first 100 ns) is roughly 0.7 mV (RMS). Fig. 3.18(c & d) proves what is indicated in the example from fig. 3.17(b), which is that the first 500 SPs have a lower baseline noise compared to all 1024 SPs. The relative high V1742 baseline noise of 1 mV (RMS) is partly caused by the VC-method (CAEN-VC), but mainly depends on the V1742 trigger rate and f_{SCA}. Lowering both factors results in baseline noises of around 0.4 mV (σ) as shown fig. 3.18(c). Lowering only the trigger rate but running the V1742 at the highest f_{SCA} of 5 GSPS, results in around 0.45 mV (σ). Thus, the main noise source is a high trigger rate for the V1742. The DT5742 measurement is less sensitive to the trigger rate which is related to the reduced data transfer speed, caused by the utilized USB2.0 connection. All measurements with the V1742 have been performed with the (faster) optical fiber connection. Summarized, the DT5742 & V1742 baselines look identical when running the V1742 at low trigger rates.

When applying the NEW-VC instead of the CAEN-VC to the X742, the baseline noise improves and is comparable to the baseline noise of the V3. The VC5 algorithm is missing in the CAEN-VC and thus for all X742 boards. The time resolution limit, that can be achieved when combining the CAEN-VC with the NEW-TC, is around 5 ps (σ) as summarized in row #13 of table 3.12. If NO-VC is applied to the X742, the time resolution is larger than 50 ps (σ) independent of the applied TC-method as listed in row #21 of table 3.13. Thus, VC1 which is the only reliable correction of the CAEN-VC is mandatory for all DRS4-chips. The best possible time resolution for the V1742 lies below 3 ps (σ), which is also the best DRS4-result among all DRS4-based boards. In this case the utilized calibration methods are the NEW-TC and the NEW-VC combined with the VC5 as summarized in row #20 of table 3.13. The investigated and re-calibrated V1742 exhibits a SCA-based board with 32 channels and a time resolution across all channels better than 3 ps (σ), independent of the measured signal delays. Other readout electronics with comparable performance are based on flash ADCs and therefore several orders of magnitude higher with respect to costs and power consumption. For comparison reasons a 2-points linear interpolation

is used to achieve the mentioned time resolution of 3 ps. Time resolutions below 1 ps (σ) become available with the DRS4 when more sophisticated analyzing techniques are applied, like the cross-correlation method. Details are found in section 4.7.

4.3 DRS4 Comparison of all TC-Methods

The comparison of the TC-methods was made with an f_{SCA} of 5 GSPS which corresponds to sampling intervals of 200 ps ($\Delta\bar{t}_b$ =200 ps). This comparison discusses exclusively the results of the P-tests. The P-test measures the fluctuation of an applied sine wave period for the individual TC-methods (details in section 2.5.1). Other sampling speeds are discussed in section 4.4.

When considering equidistant sampling intervals (NO-TC $\Rightarrow \Delta\bar{t}_b = 200\pm0$ ps), time resolutions between 100-700 ps are measured as shown in fig. 3.2. The worst results are achieved for delays around 100 ns. This result is explained by the fact that 100 ns is half of the T_{SCA} which predicts the highest variety of measured delays for a true delay of 100 ns. Although the huge timing error of NO-TC was understood, the V3-TC results in almost equidistant sampling intervals ($\Delta\bar{t}_b = 200\pm3$ ps). Nevertheless, the small modification of σ from 0 ps to 3 ps already improves the DRS4 in the V3 board to a randomly fluctuating time resolution between 35-50 ps as illustrated in fig. 3.3. Instead of this fluctuating time resolution, a constant time resolution is expected when variating the delay. Also, most timing histograms do not correspond to a Gaussian distribution like in fig. 3.3(c). The CAEN-TC provides improved timing histograms and also results in a better time resolution between $21-32$ ps. However, similar to the V3-TC, the resolution results of the CAEN-TC are randomly fluctuating depending on the delay and both methods provide the same TC table consisting of $\Delta\bar{t}_b = 200\pm3$ ps. Consequently, this indicates that both methods utilize a similar algorithm. The SP-test in fig. 3.4(b) and fig. 3.21 returns the initial frequencies of the f_{TC} for both methods, which is 50 MHz for CAEN-TC and 60 MHz for the V3-TC. This is another indication that a similar algorithm is used for both methods and additionally that both TC outcomes are over-trained. Since the CAEN-TC performs better compared to the V3-TC, although both applied al-

gorithms seem to be identical, the reason must be hardware related. The three hardware differences will be addressed in decreasing significance. First, the internal FPGA-based 240 MHz clock which was originally utilized for the V3-TC has a time jitter around 120 ps. Also, its corresponding P-test distribution (1st period or delay ≈4.17 ns) is not Gaussian. The shape is quasi Gaussian with a 20-30 ps shifted peak and a spread of more than 200 ps. Second, as already mentioned in section 4.1 the true f_{SCA} differs from the expected f_{SCA} of around 0.01 %. And third, the two-state-effect which is shown in fig. 3.1. It is caused by a 2.5 MHz digital signal on the *Printed Circuit Board* (PCB) trace close to the DRS4 chip. It induces a PLL instability inside the DRS4 which leads to two distinguishable alternating sampling speeds. A redesign of the PCB by PSI fixed the three mentioned problems and resulted in the V5.

Following are the two software reasons why the old algorithms (CAEN-TC & V3-TC) result in inferior time resolution compared to the NEW-TCs. First, in reality the $\Delta\bar{t}_b$ follows 200±74 ps and not ±3 ps as predicted by CAEN-TC & V3-TC. The huge standard deviation value of 74 ps is caused by an alternating behavior of the Δt_b (see table 3.9). One can visualize the alternating behavior with a digitized sine wave applied to X742 (CAEN-TC) where equidistant 200 ps sampling points are computed. Although the x-axis is kept equidistant, the SPs in fig. 3.16 do not show an equidistant behavior. Instead an alternating behavior is indicated which proves that the cell positions are not corrected in time due to the wrong TC algorithm. Summarized, both the CAEN-TC and the V3-TC correct the *Integral Nonlinearity* (INL) relatively well but completely fail for the DNL as illustrated in fig. 3.28. Second, all nine DRS4-channels have to be calibrated individually in time. A single channel calibration applied to the other channels limits the time resolution to around 13 ps. Proof is available in fig. 3.24(e) or table 3.13(row #13 − row #16). Both mentioned software reasons applied improve the time solution to around 3 ps (σ). This is a factor of 15 compared to the V3-TC.

All developed NEW-TCs (LTC, GTC or FTC) or dedicated combinations of the NEW-TCs will result in a time resolution around the mentioned region of 3 ps as summarized in table 3.7. However, there are minor differences which will be dis-

cussed further in this section. The LTC+3GTC is chosen as a reference TC-method. The LTC+3GTC is an algorithm that calibrates the DRS4 very robust and fast if the right parameters are chosen. The theoretical background of the LTC+3GTC is provided in section 2.2.7 and its convincing performance is demonstrated in fig. 3.24, fig. 3.25(a), fig. 3.26 and fig. 3.29. A time resolution of around 3 ps was achieved in all examples for the 100 MHz P-test.

However, the most reliable and best applicable NEW-TC is the FTC. It also provides the best performance in terms of time resolution as a result of the higher amount of statistics compared to the other NEW-TCs. In contrast, the FTC requires expensive hardware to produce the different TC frequencies and the C-code is tedious to reproduce. All utilized FTCs in this work always result in the same TC outcome because the system of linear equations is solved analytically. It should be noticed that more than three years passed between the day that the FTC frequencies are digitized and the day that the control frequency (100 MHz) is digitized for the P-test. One should also notice that all waveforms are accepted for the FTC algorithm because the two-state-effect separation is not available. The 100 MHz LTC+3GTC works best for the 100 MHz P-test as shown in fig. 3.26(c). This outcome is predictable since the same waveforms are used for the P-test and the TC-method. Thus, it is possible that the LTC+3GTC outcome is over-trained for multiples of 10 ns. Other explanations are given further down where a similar case is discussed (217 MHz LTC+3GTC @ 100 MHz P-test). One can further see in fig. 3.26(c) that fewer FTC frequencies result in a worse performance for the P-test. The performance drop from 11 to 4 frequencies is disproportional compared to the drop from 43 to 11 frequencies. The drop difference is predictable because the DNL of the digitization produces more corrupt measurements that cannot be compensated with statistics. However, the best FTC performances are achieved with 43 frequencies. The performance with more voltage levels is slightly better. This can be explained because more statistic is available for the 101-levels-case compared to the one-level-case. When looking at the 11 frequencies FTC, more voltage levels will result in disproportionately better TC performance. The explanation cannot be found in fig. 3.26(c), but is indicated in fig. 3.26(d). The 11 frequencies FTC with

101 levels shows a falling offset curve. This behavior is identical to fig. 3.29(b) where the two-state-effect causes a different sampling speed. Thus, the system of linear equations (11 frequencies FTC with 101 levels) is solved for the sampling speed of the right state. In other words, depending on the starting conditions of the FTC, the same (correct) sampling speed will always result, which are two candidates in case of the V3. For the given FTC examples in fig. 3.26(c & d), the right state TC is computed only once and in the other cases the left state TC. Thus, a superposition of both states was never computed. This is even more impressive considering the fact that the two-state-effect was not actively rejected for the FTC. One should also mention that the f_{SCA} of the DRS4 stays constant over time as illustrated in the three years younger 100 MHz P-test (left state). When applying the LTC+3GTC to the old dataset of two FTC frequencies (217 MHz & 239 MHz), the FTC performs slightly better in all cases. Interestingly, the time resolution in fig. 3.26(e) results in two distinguishable oscillating curves which depend on the P-test frequency. The oscillating curves are caused by the imperfection of the signal generator which utilizes an internal clock with a given time jitter to generate the TC sine wave signals. When taking a closer look at identical looking oscillating curve shapes in fig. 3.26(e), for example the 239 MHz P-test, the 43 frequencies FTC results in a slightly better time resolution compared to the 217 MHz LTC+3GTC. The 100 MHz LTC+3GTC also provides the mentioned curve shapes but results in inferior performance with regards to offset and timing compared to all other methods. Its performance degradation can be addressed by four reasons. First, a 100 MHz sine provides less statistics for the TC compared to the 217 MHz sine. This argument becomes clearer when looking at the simulation in fig. 2.11(a). One can see that a single waveform has around five times more GTC corrections (217 MHz vs. 100 MHz) because of the increased amount of available $\Delta t_{a,b}$ (n_{all}). Second, when analyzing (1.17) one can predict that the time resolution for a single linear interpolation is better for a faster TC frequency. In this particular 5.12 GSPS case, one can predict based on fig. 2.11(d) that the expected time resolution improvement for the 217 MHz interpolation is approximately double compared to the 100 MHz interpolation. Four measurements are

necessary to achieve a 2 times better SNR[V]. Thus, the theoretical available $\Delta t_{a,b}$ increases when including the first reason to a factor of 20 for an f_{TC}-change from 100 MHz to 217 MHz. Third, the DRS4 temperature was not recorded three years ago so the board temperatures could have shifted. The effect of the DRS4 temperature is discussed in section 4.4. Fourth, the two-state-effect is not correctable for the 3 years old dataset. The above mentioned reason (100 MHz LTC+3GTC @ 100 MHz P-test), where an over-training is named as a possible explanation for the superior performance of the LTC+3GTC compared to the FTC is invalidated with the results in fig. 3.26(e). This is because both TC frequencies (217 MHz & 239 MHz) result in reduced performance compared to the FTC independent of the chosen P-test frequency. The result also proves that the FTC is the best TC-method among all NEW-TCs.

The LTC+3GTC combines two NEW-TCs, the LTC and the GTC. Both can also be applied successfully as standalone methods if the correct modifications are used. Two requirements are mandatory for a reliable standalone LTC which are a low f_{TC} and the correct f_{SCA} information. If the wrong f_{SCA} is used, as it was the case for the V3, a systematic delay error results as illustrated in fig. 3.26(b). The other requirement of a low f_{TC} is demonstrated by increasing the f_{TC} in fig. 3.26(a). One can see that the lowest f_{TC} (30 MHz) results in the best TC outcome among the standalone LTCs. This is caused by two factors. First, the individual DRS4 cells have different bandwidths. One can extract two bandwidth regions which are distributed along the 1024 DRS4 cells as visualized in fig. 3.27(a). Second, the linear interpolation fails for sine waves with a high f_{TC}. It results in systematic errors as simulated in fig. 2.11(f) and demonstrated for an f_{TC}=239 MHz in fig. 3.27(c & d). Summarized, a standalone LTC can reach comparable results to that of the LTC+3GTC. The performance will be sightly reduced but the computing time is faster (see table 3.7).

The standalone GTC needs around 2 minutes (see table 3.7) to perform an accurate TC. Both algorithms (GTC and V3-TC) function similarly when looking at the C-code of the V3-TC from PSI. One could argue that the V3-TC which is

[V]Identical to the illustrated fraction in (1.17), the SNR in this work is calculated by dividing the absolute amplitude by the σ of the baseline noise.

applied for a few seconds performs equally if the computing time is also increased to 2 minutes. But this is not the case. What clearly separates the developed GTC from the V3-TC is that the GTC only corrects the Δt_b inside the measured period, whereas the V3-TC corrects all Δt_b each time a period is measured. Thus, it does not allow the f_{SCA} to be changed during the calibration process, which is mandatory for a successful TC. Even if the true f_{SCA} is known, the f_{SCA} must fluctuate continuously hundreds of ps during the calibration process making corrections and finally arriving at the expected f_{SCA}. If the expected f_{SCA} is not recovered, the GTC fails. In the V3 case the GTC only seemed to fail but instead the true f_{SCA} became available because of the GTC (see table 3.6). However, it is tedious to apply the standalone GTC for three reasons. First, a successful standalone GTC outcome requires the longest computing time. Second, if a too long a computing time is chosen and no abort-routine is implemented the TC outcome will be over-trained as illustrated in fig. 3.25. Particularly fig. 3.25(c) shows the TC frequency of 100 MHz as a systematical error inside the TC outcome. Third, a negative Δt_b can only be measured if error-prone GTC settings are chosen as shown in fig. 3.25(d). The three mentioned reasons can be ignored if the GTC is combined with the LTC (e.g. LTC+3GTC, details in section 2.2.7). What cannot be ignored is the f_{SCA} fluctuation when applying the GTC multiple times as visualized in fig. 3.27(f). The mentioned fluctuation of the DRS4 causes a linearly increasing error which is dependent on the measured delay. This behavior is clearly visible in all P-tests. For example in fig. 3.24(a) the time resolution for almost no delays is 3 ps but increases to around 5 ps for the maximum delay. Thus, the DRS4 fluctuation is 4 ps ($\sqrt{5^2 - 3^2}$) for an f_{SCA}= 5 GSPS. An explanation for the DRS4 fluctuation is given by Stricker-Shaver et al [31]. The DRS4 fluctuation for other sampling speeds is covered in section 4.4.

Summarized, the LTC+3GTC provides the best compromise with respect to required TC hardware, TC performance, computing time and reproducibility. PSI adopted one combination of the NEW-TCs, the V5-TC, which performs equally compared to the NEW-TCs for the tested f_{SCA} of 5.12 GSPS (see section 4.5). The theoretical DRS4 performance is accomplished at last with all NEW-TCs and enables

a time resolution below 1 ps. A deeper discussion concerning the 1 ps measurement is provided in section 4.7.

4.4 DRS4 Performance for Different Parameters

Discussed in this section are five DRS4 parameters separated by paragraphs. The following five parameters are the DRS4 fluctuation, the alternating Δt_b behavior, the channel dependent TC, the two-state-effect and the DRS4 temperature behavior of the V3 for different sampling frequencies. The three addressed sampling frequencies are 5 GSPS, 2 GSPS and 1 GSPS.

First, as mentioned in the previous section 4.3 the time resolution decreases linearly to around 2 ps/100 ns (σ) at 5 GSPS due to the f_{SCA} fluctuation of the DRS4. The same effect is illustrated for other sampling speeds in table 4.2. One can see that the time resolution degradation versus a fix delay worsens proportionally with the inverse of the f_{SCA}.

Table 4.2: Listed is the measured linearly decreasing time resolution (σ loss) of three f_{SCA} for the DRS4-chip. Used are two delay points from the 100 MHz P-test, the shortest (best σ) and the longest delay (worst σ).

f_{SCA}	best σ	worst σ	σ loss	source
5 GSPS	≈3 ps	≈5 ps	$\frac{\approx 2\,\text{ps}}{100\,\text{ns}}$	fig. 3.24(a)
2 GSPS	≈5 ps	≈30 ps	$\frac{\approx 6\,\text{ps}}{100\,\text{ns}}$	fig. 3.31(a)
1 GSPS	≈20 ps	≈130 ps	$\frac{\approx 13\,\text{ps}}{100\,\text{ns}}$	fig. 3.32(a)

Second, the DRS4 shows an alternating behavior as presented in table 3.8. One can predict for a high f_{SCA} of 5 GSPS the behavior as 270 ps for even Δt_b and 130 ps for odd Δt_b with a σ around 23 ps. When taking a closer look at the Δt_b distribution in fig. 3.25(d), the Δt_b behavior is further separable in a first and a second half, whereas the second half shows a stronger separation and alternates between 280 ps and 120 ps. The first half alternates between 260 ps and 140 ps. With the separation in four alternating regions, the σ decreases to around 17 ps for a region. Also visible

in table 3.9 is that σ increases when increasing the f_{SCA}. Additionally, at 1 GSPS the alternating behavior is almost equidistant due to is relativity high σ of around 230 ps. Summarized, the developers of the DRS4 expected a one order of magnitude lower Δt_b behavior compared to the true Δt_b behavior (see table 3.9). Also mentionable are the extrema of the Δt_b which spread from a negative value up to a doubling of the expected sampling interval. A negative Δt_b means that a signal will arrive earlier in the following SP compared to the momentary SP. Only Δt_{499} can be negative and ranges between -20 ps and 50 ps at 5.12 GSPS. This number results from the experience of around 30 calibrated DRS4-chips. The other extrema are summarized in table 3.8 and table 3.9.

Third, the time resolution degrades in all f_{SCA} cases if a channel-dependent TC is not performed. Examples are shown in fig. 3.30 and fig. 3.24(e). When comparing fig. 3.30(b) with fig. 3.24(e), a slow f_{SCA} seems to have less degradation compared to a fast f_{SCA}. In fact, when applying (1.14) one will calculate consistently a 13 ps (σ) degradation for all three f_{SCA} cases independent of the delay.

Fourth, the two-state-effect results in two distinguishable sampling speeds for all three preset f_{SCA}. The examples in fig. 3.29(b & f), fig. 3.31(b) and fig. 3.32(b) confirm the offset results in table 3.6 (column "State Offset"). In particular, the TC of the right state causes a negative offset trend when applied to waveforms that origin from the left state. The offset behaviors in fig. 3.29(b) indicate that waveforms from the left state are digitized with a faster sampling speed compared to waveforms from the right state. The time resolution also degrades if the wrong state is used for the TC for all three f_{SCA}. It degrades especially for delays around $\frac{T_{SCA}}{2}$ when compared to the expected time resolution as illustrated in fig. 3.29(a & e), fig. 3.31(a) and fig. 3.32(a).

Fifth, DRS4-temperature changes can have a big impact on the time resolution behavior as shown in fig. 3.29(e), fig. 3.31(a) and fig. 3.32(a). Shown is a time resolution spread from 4 ps to 20 ps at 5 GSPS for extreme temperature jumps. The biggest impact on the degradation for all f_{SCA} happens for delays around $\frac{T_{SCA}}{2}$ which is similar to the before mentioned two-state-effect. Therefore, the two-state-effect combined with a huge temperature jump further degrades the time resolution as

illustrated in fig. 3.29(e). The impact on the time resolution is negligible if the temperature fluctuates 1-2 °C as demonstrated in fig. 3.29(c). Temperature jumps have no measurable effect on the f_{SCA}. The influence of temperature changes for certain $\Delta t_{a,b}$ are illustrated fig. 3.29(d) . One can see that some $\Delta t_{a,b}$, like $\Delta t_{1,100}$, drift dramatically in time when the DRS4-temperature is changing. However, when adding individual $\Delta t_{a,b}$ together to receive a full DRS4 rotation ($\Delta t_{700,200}+\Delta t_{200,700}$), no time drift is measurable which proves that the preset f_{SCA} is stable over a wide temperature range.

4.5 DRS4 vs. Other Readout Electronics

This section mainly discusses table 3.12 where the results of the same SP-test applied to all introduced readout electronics are summarized. A two-point LED is used for digital devices which provides an easy comparison to an analog LED. Further, a similar dynamic range of around 1 V peak-to-peak is utilized across all devices.

Naturally, at the beginning of this work, the DRS4 (V3 or X742) was compared with an available oscilloscope which was the S5. Both DRS4-based boards provide a higher acquisition rate than the S5 because the S5 requires a long preprocessing time and thus the ADC-based S5 shows no speed advantage. Advantageous for the S5 is the build-in amplifier which enables the user to operate in a chosen dynamic range. On the other hand the V3 is one order of magnitude less expensive compared to the oscilloscope, less bulky and easily fits inside a pocket. However, both oscilloscopes (S5 or S20) showed higher baseline noises independent of the amplifier settings compared to the DRS4 noise which is less than 0.4 mV. Since the DRS4 offers 12 bits and the S5 only 8 bits, only signals greater than 1 V can take advantage of the build-in amplifier. The V3 cannot be utilized when working with slow signals because it only ranges from 0.7 GSPS to 5 GSPS. A comparison between the X742 and the S5 when running both at the fastest sampling speed of 5 GSPS results in an equal time resolution as shown in row #7 vs. row #18. This is a surprising outcome since the bit-resolution is far worse for the S5 (8 bit vs. 12 bit). Twice as surprising is the comparison between the V3 and the S5 which degrades the DRS4-results

further to a factor of 2 (row #4 vs. row #18). When looking in table 3.13 where the measured time resolution (7^{th} column) is compared to the theoretical time resolution (8^{th} column), the expected DRS4-performance is achieved once the correct DRS4-calibrations (NEW-TC) are applied [VI].

The DRS4 in combination with the NEW-TC will be used exclusively as reference in the remaining section. The V5-TC which is an extraction of the NEW-TC performs similarly for the V5 according to table 3.12. A better comparison in table 3.13(row #17 vs. row #18) reveals the best time resolution accomplished with the NEW-TC. The improvements are minor and thus the V5 performance is also very satisfactory for fast sampling speeds. The chosen f_{TC} of 100 MHz in the V5 cannot calibrate accurately all sampling speeds (0.7 GSPS to 5 GSPS) as reproducible with (2.26). Considering this, an f_{TC} of around 70 MHz would have been the most flexible. In general an f_{TC} of $\frac{1}{20} \cdot f_{SCA}$ is the easiest to implement when utilizing the NEW-TC. Thus, an f_{TC} of around 35 MHz for 0.7 GSPS.

Last, the DRS4 is compared to analog readout electronics. The results are available in table 3.15. In some of these measurements the DRS4 is utilized together with the investigated analog devices and therefore the DRS4 error is subtracted afterwards. The resulting performance table 3.12(row #19 − row #22) shows that the DRS4 (3 ps) is superior compared to the NIM-LED (4 ps) and the NIM-CFD (6 ps). However, these devices are usually used in combination with a secondary timing device, like a TDCs or the NIM-TAC. The best achievable NIM-TAC performance is around 11 ps when using a 14 bit ADC. This result shows that a digital solution, like the DRS4, provides a lot of opportunities for improving signal processing and performs even better than the well-established analog solutions.

4.6 Time Resolution Prediction for the P-Test

The P-test is the key method for evaluating the SCA technology. The three possibilities to apply the P-test are described in section 2.5.1.

The 1^{st} possibility can only test one specific delay very accurately and should

[VI] A detailed discussion of precisely predicting the DRS4 time resolution can be found in section 4.6

always result in a Gaussian histogram. Its results are included in the 2nd possibility of the P-test which is discussed later. The 1st possibility is rarely used in this work and then mostly if the measured distribution is not Gaussian in nature. This is generally the case when measuring with wrongly calibrated DRS4 like in fig. 3.3.

The 2nd possibility has 5 features which have been applied continuously in this work. First, this P-test provides fast and easy feedback of how efficient a TC-method works. Second, it offers comparison capabilities between individual TC-methods. Third, one can directly measure a frequency offset and thus it provides the true frequency, e.g. the f_{SCA} or the f_{TC}. Fourth, one can evaluate the time resolution of individual readout electronics. Fifth, one can roughly predict the time resolution of any analog signal (at a given delay) in combination with any readout electronics, for example the DRS4. A simplified approach is already published by Stricker-Shaver et al[31] speculating that the DRS4 time resolution is degrading inversely with the sampling frequency. However, the results of the different P-test scenarios led to a better prediction. It has already been partially summarized in table 4.2 and will be further demonstrated in the following lines.

The time resolution of the P-test is dependent on six error sources which can be unfolded with (1.14). The 1st error refers to the quality of the TC-method. All NEW-TCs, especially the FTC, provide errors close to 0 ps (σ) if applied correctly. An example is available in fig. 3.24(c), where a better TC outcome is provided by the f_{TC}=100 MHz compared to the f_{TC}=66 MHz. This is caused by the statistical limitations of the 66 MHz clock which is synchronized to the DRS4-chip and therefore results in a decreased NEW-TC outcome. The 2nd error arises from the f_{SCA} inconstancy as described in table 4.2. One can see that the DRS4 fluctuates around $\pm$2 ps for an f_{SCA} of 5.12 GHz. When analyzing fig. 3.24(c) one can also calculate this 2nd error independently from the 4 illustrated curves. The 2nd error is a linear function of the delay and always results in an error increase of around 2 ps/100 ns. The first two described errors are only of relevance for an SCA whereas the 3rd and all following errors also cover digital readout electronics. The 3rd error is caused by the time jitter of two adjacent cells of an SCA. For ADCs, the 3rd error is the time jitter of a single cell which samples continuously. Specifically, the opening time and

the closing time of a cell that in turn will collect charge must happen exactly at the same time points compared to previous charge collections. The design of the DRS4-chip is optimized for a fast f_{SCA}, therefore the last two decribed errors grow when lowering the sampling speed. In table 4.3 one can find both errors which have been calculated with the results in section 3.3.1 and section 3.3.2. The 4^{th} error

Table 4.3: Listed is the linearly decreasing time resolution (2^{nd} error) of three f_{SCA} for the DRS4-chip. Additionally listed is the 3^{rd} error which represents a permanent error for the time resolution.

f_{SCA}	2^{nd} error	3^{rd} error	source
5 GSPS	$\approx 2\,\text{ps}/100\,\text{ns}$	$\approx$1 ps	fig. 3.24(a)
2 GSPS	$\approx 6\,\text{ps}/100\,\text{ns}$	$\approx$4 ps	fig. 3.31(a)
1 GSPS	$\approx 13\,\text{ps}/100\,\text{ns}$	$\approx$15 ps	fig. 3.32(a)

describes the combination of all voltage fluctuations. It is typically given as baseline noise of the system and 0.37 mV for the DRS4-chip. Note that a baseline noise will increase the moment an input signal is connected. The 5^{th} error is dependent on the analyzing method (e.g digital LED or cross-correlation) utilized. For example a basic 2-points digital LED can be described by (1.17). Not considered in (1.17) is the δ_{lin} caused by sine waves without perfect linear behaving edges. δ_{lin} increases with longer sampling intervals and is simulated in fig. 2.11(e & f). Note that the δ_{lin} represents a maximum error. The five previously introduced errors are standard deviations (σ). The 6^{th} error which is also described by σ is correlated to the mentioned δ_{lin}. A significant 6^{th} error is expected for a 100 MHz P-test with an f_{SCA} of 1 GSPS ($\Delta t_b \in [0.2\,\text{ns}, 1.8\,\text{ns}]$) because the plotted rise times fluctuate around 20% as shown in fig. 2.11(c). For this reason the 6^{th} error is experimentally measured for an f_{SCA} of 1 GSPS in fig. 3.32(a) where the 30 MHz P-test provides an approximately 13 ps better time resolution compared to the 100 MHz P-test (explanation follows). Without the 6^{th} error one would expect the opposite outcome similar to fig. 3.31(a) where the 100 MHz P-test performs better than the 30 MHz P-test. After this introduction an example to predict the P-test outcome is given in the following

lines.

The 1st error can be excluded because the error caused by the NEW-TC is negligible. The 6th error can be excluded if a slow P-test frequency like 30 MHz is considered. A 30 MHz sine wave is linearly rising around 9.4 mV/100 ps as shown in fig. 2.11(d). The remaining four errors are linked together and can be separated in two error pairs. First, when considering a 2-points LED the problem becomes describable with (1.17). In this case the σ_u in (1.17) is the 4th error representing the baseline noise. The σ_u of the DRS4-chip is expected to be around 0.37 mV. From the measurements a σ_u of 0.5 mV is more realistic which includes the noise of the signal. The error from the 2-points LED must be doubled for the P-test because a delay between two edges is calculated. With the just introduced numbers and (1.17) one can predict the 5th error which includes the 4th error. The resulting LED outcome is around 7.5 ps ($= \frac{0.5\,\mathrm{mV}}{9.4\,\mathrm{mV}} \cdot 100\,\mathrm{ps} \cdot \sqrt{2}$). Second, this LED prediction is further processed to predict the time resolution of the P-test by adding both DRS4 errors from table 4.3. Thus a delay of 170 ns at 5 GSPS results in $\sqrt{(1\,\mathrm{ps} + 170\,\mathrm{ns} \cdot 2\,\mathrm{ps}/100\,\mathrm{ns})^2 + (7.5\,\mathrm{ps})^2} \approx 9\,\mathrm{ps}$ which is exactly the measurement outcome in fig. 3.24(a). More P-test predictions are compared to its P-test results in table 4.4. One can see that most predictions do not differ more than 1 ps from the

Table 4.4: Listed are two P-tests (30 MHz & 100 MHz) of three f_{SCA} for the DRS4-chip. The theoretical standard deviation is additionally illustrated in brackets.

P-test frequency	f_{SCA}	delay ≈ 30 ns	delay ≈ 170 ns	source
30 MHz	5 GSPS	≈8 ps[8]	≈9 ps[9]	fig. 3.24(a)
30 MHz	2 GSPS	≈10 ps[10]	≈17 ps[16]	fig. 3.31(a)
30 MHz	1 GSPS	≈21 ps[20]	≈37 ps[38]	fig. 3.32(a)
100 MHz	5 GSPS	≈3 ps[3]	≈5 ps[5]	fig. 3.24(a)
100 MHz	2 GSPS	≈7 ps[6]	≈14 ps[14]	fig. 3.31(a)
100 MHz	1 GSPS	≈23 ps[19]	≈40 ps[37]	fig. 3.32(a)

measured time resolutions. The exception is the 1 GSPS case applied to the 100 MHz P-test where the theory is 4 ps lower than the measurement. This exception is caused

by the 6$^{\text{th}}$ error which was not considered at the beginning of the paragraph. Also the 6$^{\text{th}}$ error is not 4 ps (=23 ps−19 ps) lower, but 13 ps ($\approx \sqrt{23^2 - 19^2}$) due to (1.14). This matches well to the experimentally measured 6$^{\text{th}}$ error of 13 ps[VII].

Summarized, the P-test is an essential tool for the SCA technology and for testing individual readout electronics. However, the P-test is restricted only to one channel. Since at least two channels are needed in most applications to perform a time resolution measurement a more advanced performance test is required, the SP-test.

4.7 Best DRS4 Time Resolution for the SP-Test

The SP-test was originally utilized in this work to understand the influence of readout electronics for PET-measurements. It was discovered that the DRS4 performs adequately (≈100 ps FWHM) for preclinical PET-applications where the common CRT lies around 1 ns (FWHM). However, the poor DRS4 time resolution and its fluctuation with the delay gave birth to the NEW-TC which solved these time resolution problems (summarized in fig. 4.1).

Finally, the NEW-TC established the full performance of the DRS4[VIII] which lies below 2 ps (FWHM) or 0.8 ps (σ) as shown in fig. 1.4.

One can predict the outcome of the SP-test identically to the P-test in section 4.6. This is especially useful for synchronizing multiple DRS4-chips. Before discussing multiple DRS4-chips, the SP-test for a single DRS4 will be predicted. The utilized SP-test in section 3.3.3 consists of a split signal with the same rise time (60 mV/200 ps) compared to the 100 MHz P-test which is simulated in fig. 2.11(d). Thus, the same time resolution is expected for a 2-points LED (for equal delays). According to section 4.6, the theoretical 2-points LED for no delay results in $\sqrt{(1\,\text{ps} + 0\,\text{ns} \cdot 2\,\text{ps}/100\,\text{ns})^2 + (2.3\,\text{ps})^2} \approx 2.5\,\text{ps}$ (σ). This is roughly the same time resolution as measured in fig. 3.34(a) for the 2-points LED. Thus, the theoretical

[VII] For the 13 ps calculation a linear fit is applied to both bottom P-tests in fig. 3.32(a) resulting in 20 ps (100 MHz) and 17.5 ps (30 MHz) for no delay. Additionally, the 5$^{\text{th}}$ error (2-points LED) 2.3 ps (100 MHz) and 7.5 ps (30 MHz) is subtracted. Finally, the 6$^{\text{th}}$ error is calculated as 13 ps ≈ $\sqrt{(20^2 - 2.3^2) - (17.5^2 - 7.5^2)}\,ps$.

[VIII] The SP-test was the key method to evaluate the theory of the channel-dependent TC which is described in section 2.2.10.

approach from the P-test (section 4.6) also works to predict the SP-test results.

When comparing the 50 ns delay of the 2-points LED with the 6-points LED as illustrated in fig. 3.34(c vs. d) one can calculate that 4 additional SPs improve the time resolution around 2 ps ($\approx \sqrt{3.2^2 - 2.5^2}$). An improvement was expected since more SPs have been utilized. To predict the time resolution of this SP-test, the equation that describes the 5^{th} error must be modified. Also the 3^{rd} error in table 4.3 must be calculated more accurately. This is especially the case when the predicted time resolution improves below 1 ps (σ).

One of the best time resolutions of this work with 0.9 ps (σ) is illustrated in fig. 3.34(b). It is also mentioned by Stricker-Shaver et al[31] but not shown. It is still the best time resolution that was ever published for an SCA. The ICC which uses 50 points of the split signal was utilized to accomplish the 0.9 ps. When repeating this SP-test for a delay of 50 ns, the time resolution degrades to 1.8 ps which supports the investigated error of 2 ps/100 ns discussed in section 4.6. The dedicated distribution is shown in fig. 3.34(e) where an extension of the Gaussian distribution can be seen. Temperature fluctuation is the explanation for this extension. The SP-test measurements and the NEW-TC were performed on different days. The DRS4 must be temperature stabilized for time resolution measurements below 1 ps (σ). The same temperature phenomena is already discussed in section 4.4 where a temperature jump will result in a degradation of the time resolution as a function of the delay.

A split oscillating signal is mandatory for synchronizing two DRS4-chips. A 100 MHz sine wave is used for this purpose (see fig. 3.33). One can understand from fig. 3.35(f) that without the oscillating signal the time resolution between two PSI boards is around 1.2 ns. The resulting time resolution of the 4 involved signals is predicable by the two experiments that have already been discussed before. First, the 100 MHz P-test which is discussed in section 4.6 resulted in around 3 ps (σ). Second, the 2-points LED from the beginning of this section resulted in around 2.5 ps (σ). Thus, a time resolution of around 3.9 ps ($\approx \sqrt{3^2 + 2.5^2}$) is expected if two 2-points LEDs are applied to the 4 digitized signals. With the measured 4.1 ps (σ), the theory is close to the result in fig. 3.35(c). Fig. 3.35(a – d) also shows that

the oscillating signal has a higher time error compared to the split pulse as expected. A 6-points LED can synchronize two DRS4-chips below 2.9 ps (σ), which is a single time resolution of around 2.0 ps. This is impressively shown in fig. 3.35(e) where the other DSR4-chip was stopped 160 ns later with no significant time resolution degradation. The same result is also visible for other delays in fig. 3.34(a) when looking at the curve consisting of triangles. The other SP-test in fig. 3.34(a) show a linearly decreasing time resolution as predicted in the previous section 4.6. Thus, the oscillating signal compensates additionally the fluctuation of the preset f_{SCA} (2^{nd} error).

The remaining SP-test results are discussed in the previous section 4.5 where the DRS4 is compared to other readout electronics. A superficial overview of all applied SP-tests is provided in table 3.12.

4.8 CRT-Test with the APD-Based PET-INSERT

The old time calibration (V3-TC) that came with the V3 board was used for the CRT-test with the PET-INSERT (see results in section 3.1.6). The Quicksilver electronics from Siemens predetermines the CRT to more than 4 ns (FWHM), which is far more than the expected error resulting from the V3-TC of around 400 ps (see row #6 & 12 in table 3.12). The degradation caused by the V3-TC is less than 20 ps (4 ns vs. $\sqrt{4000^2 - 400^2 + 71^2}$ ps) for this experiment due to (1.14). Thus, the V3-TC has an insignificant effect on the following CRT-test discussion.

When analyzing table 3.2, one can see that an LED with no walk correction results in the worst CRT of 9.4 ns (FWHM). The 9.4 ns required additionally the lowest available TH of 8 mV as shown in fig. 3.14(a). The low TH was predictable since the absence of a walk correction can only be compensated by measuring the arrival time at a low TH. This is especially the case for a maximum EW which includes the Compton continuum and the complete photo-peak. Therefore, higher PET energies (EW $>$ photo-peak) result in an improved CRT of 2.9 ns (FWHM). The effect is highlighted between row #1 (9.5 ns) and row #3 (2.9 ns). The CRT improvement in row #3 is achieved by rejecting 99% of the PET-events. The same effect but with

an improved CRT is visible if a walk correction is additionally applied. One can observe the strength of the walk correction in table 3.2, where the CRT improves from 9.5 ns (row #1) to 4.4 ns (row #4). The corresponding 2D-matrices for both mentioned rows are available in fig. 3.14(a & c). This walk correction also works inside the MF, but the MF degrades the CRT to around 4.7 ns (FWHM) (row #4 vs. row #12). Two 2D-matrix examples for the MF measurements are given in fig. 3.14(e & f) which correspond to row #14 and row #15. The two 2D-matrices emphasize that higher PET energies cause less improvement with respect to CRT compared to the measurements outside the MF. Table 3.2 also demonstrates that a spline fit shows almost no CRT improvement compared to a 2-points linear fit interpolation.

The digital CFD results in table 3.3 show again that higher PET energies result in improved CRT. Again the spline fit shows no big improvements when looking at the CRT in comparison with the 2-points linear fit interpolation. Interestingly, the CRT stays at 4.7 ns (FWHM), if all energies are allowed, for measurements inside and outside the MF (row #1 vs. row #9). Outside the MF the CRT demonstrates an improvement when narrow EWs are used (row #2). On the other hand inside the MF, the CRT is independent from the EW (row #9 vs. row #10). The best CRT is achieved for an averaged fraction of 17% when looking at the CFD settings in table 3.3. The ideal delay is shorter (around 80 ns) for a narrow EW and longer (> 100 ns) for the maximum EW. This is not the case inside the MF where a longer delay (> 100 ns) works best for all measurements.

In practice the CRT of the PET-INSERT is measured with the Quicksilver electronics and results is 4.4 ns (FWHM) outside the MF and 4.7 ns (FWHM) inside. The Quicksilver electronics consists of CFDs coupled to fast 3 GHz TDCs. It uses the crystal-map additionally to compute a crystal-to-crystal CRT, which is an advantage compared to the block-to-block CRT of the DRS4 measurement.

Summarized, a digital CFD is more stable (always around 4.7 ns) and easier to apply compared to the digital LED with walk correction for the PET-INSERT. The reason is that the fluctuating baseline caused by the MF (see fig. 3.12) is compensated by the CFD algorithm. However, the LED performs better compared to the

CFD outside the MF (4.4 ns vs. 4.7 ns) and thus is equal to the Quicksilver electronics. Consequently, one can expect from the DRS4 a further improved CRT for a crystal-to-crystal correction.

4.9 All CRT-Tests with a $3 \times 3 \times 20$ mm^3 LSO-Crystal

All photodetector results with $3 \times 3 \times 20\,\text{mm}^3$ LSO-crystals are listed in table 4.5. The APD was the slowest photodetector that was investigated in this comparison. Thus, the worst CRT was expected and also measured with around 1.2 ns (FWHM). The V3-TC causes a CRT degradation of less than 10 ps (1.2 ns vs. $\sqrt{1200^2 - 140^2 + 24^2}$ ps, see row #6 & 12 in table 3.12) and is therefore negligible.

Table 4.5: Listed are the results of three CRT-tests (APD, SiPM and PMT) coupled to a $3 \times 3 \times 20\,\text{mm}^3$ LSO-crystal when utilizing the DRS4-chip. The DRS4-chip was running at a sampling speed of 2 GSPS (APD) and 5 GSPS (other). The applied analyzing technique was a digital LED (2 points) with no walk correction. Additional information is provided in the 5^{th} column.

PET-detector	digitizer	best CRT	method	source
APD+LSO	V3 (V3-TC)	≈1.2 ns (FWHM)	LED	table 3.1
SiPM+LSO	V3 (V3-TC)	≈572 ps (FWHM)	LED	section 3.1.4
SiPM+LSO	X742 (NEW-TC)	≈560 ps (FWHM)	LED	fig. 3.40
PMT+LSO	V3 (V3-TC)	≈160-290 ps (FWHM)	LED	fig. 3.6

As expected both SiPM measurements in table 4.5 result in a better CRT compared to the APD. The same CRT-test in section 3.4.2 utilizing the DT5742 (NEW-TC) has also been evaluated in section 3.1.4 with the V3 (V3-TC). Both measurements were performed with the same bias voltage, scintillation-crystal settings and f_{SCA} but with different TC-methods. Therefore, the CRT-test outcome should be comparable except for the CRT degradation caused by the V3-TC. And indeed when utilizing (1.14) one can reproduce the V3-TC degradation which is predicted in table 3.12(row #4) as $\sqrt{572^2 - 560^2}$ ps ≈ 100 ps (FWHM). Note that this is not the

best CRT that can be achieved with this PET-detector. The photo-peak is around 200 mV for the CRT-test with SiPMs in this example. An improved CRT is possible with a better amplifier enabling the arrival time of the first photoelectrons to be computed very accurately.

Although the photo-peak of the PMTs and previous discussed SiPMs lies around 200 mV, the best CRT is expected with PMTs because of its faster rise time. The CRT has more than doubled in improvement but is dependent on the delay. A CRT of around 160 ps was measured for almost no delay and as much as 290 ps for other cases. A similar effect can also be seen for the SP-test in fig. 3.4(b) where short delays result in improved time resolution compared to long delays. Therefore the CRT degradation should not be much greater than 100 ps (FWHM) as shown in table 3.12(row #4). In this PMT scenario the CRT degradation is around 240 ps ($\sqrt{290^2 - 160^2}$ ps). Thus, an additional error must cause these multiple CRT fluctuations. A possible explanation is that the PMT measurements were not repeated exactly under the same conditions, like temperature changes, drying of the optical grease, touching or wetting the teflon tape and so forth. For this reason a constant behaving PET-detector with a similar CRT is investigated and discussed in the following section 4.10.

Summarized, the DRS4 performance is predictable with its old calibration (V3-TC) for CRTs of 500 ps (FWHM) or higher. The tested APD had the worst time resolution followed by the SiPM and PMT. Today, it is known that PMTs and SiPMs will result in equal CRT performance as described in various publications [29, 30]. This was not achieved in these CRT-tests because of the before mentioned reasons.

4.10 CRT-Test Problem with PMTs and the DRS4

The CRT for PET-measurements is greater than 100 ps (FWHM) when utilizing LSO-crystals that are longer than 5 mm as described by Vinke et al[30]. This is also the case in this CRT-test with PMTs coupled to $5 \times 5 \times 5\,\text{mm}^3$ LSO:Ca-crystals where a CRT of around 170 ps is expected. The coupling remains constant over time (see section 2.5.6) and therefore this reproducibly behaving PET-detector can

be utilized for comparison measurements.

Table 4.6: Eight CRT-tests utilizing the same PET-detector with different readout electronics. The PET-detectors consist of two fast PMTs each coupled to $5 \times 5 \times 5\,\mathrm{mm}^3$ LSO:Ca. The DRS4-chip was running at a sampling speed of 5 GSPS. The applied analyzing technique was a digital LED (2 points). Labeled with "(*)" are the cases where a walk correction was additionally performed. More information is provided in the 6^{th} column.

row	PMT-out	digitizer (info)	best CRT	method	source
1	dynode	X742 (CAEN-TC)	≈157 ps (FWHM)	LED(*)	fig. 3.23(e)
2	dynode	X742 (CAEN-TC)	≈166 ps (FWHM)	LED	fig. 3.23(f)
3	dynode	X742 (NEW-TC)	≈173 ps (FWHM)	LED(*)	fig. 3.39(e)
4	dynode	X742 (NEW-TC)	≈176 ps (FWHM)	LED	fig. 3.38(e)
5	anode	X742 (NEW-TC)	≈181 ps (FWHM)	LED(*)	fig. 3.39(f)
6	anode	X742 (NEW-TC)	≈184 ps (FWHM)	LED	fig. 3.38(f)
7	anode	S20 (5 GSPS)	≈186 ps (FWHM)	LED(*)	table 3.14(d)
8	anode	S20 (20 GSPS)	≈181 ps (FWHM)	LED(*)	table 3.14(f)

The results of these comparisons are listed in table 4.6. When applying the walk correction additionally to the LED, the CRT improves slightly (row #3 vs. row #4 or row #5 vs. row #6). The first row of table 4.6 demonstrates a 16 ps better CRT than actually even possible when applying the CAEN-TC to the DRS4 (row #1 vs. row #3). All previous measurements showed exactly the opposite behavior which is that the NEW-TC results in a better time resolution compared to the CAEN-TC. An indication that the DRS4 (NEW-TC) provides the best possible and correct CRT is shown by reproduction of the same results with the S20 in table 4.6. The S20 settings of the 5 GSPS case mimic the CRT-test of the DRS4 and result in a reduced CRT due the smaller bit-resolution (row #7). When digitizing 4 times faster, the S20 (20 GSPS) achieves the same CRT as the DRS4 (NEW-TC) with 181 ps (row #8). Additionally, when looking at the CAEN-TC measurements in fig. 3.23(a) one will find five minima instead of one (expected) minimum. Also the other delay case in fig. 3.23(b) results in a pattern (three minima) when the CRT is plotted in a 2D-matrix. The reason for this wrong result is explained in the following lines. The

sampling intervals of the CAEN-TC provides almost equidistant 200 ps sampling intervals. The true Δt_b alternates between 130 ps and 270 ps as mentioned at the beginning of chapter 4. Different delays between the two PET signals are measured when changing the TH settings (walk effect) as shown in fig. 3.23(c). The five minima also represent regions of similar delays as shown in fig. 3.23(a vs. c). When this delay is always calculated by interpolation between two neighboring cells that are 270 ps apart but wrongly considered to be 200 ps, the resulting standard deviation will be smaller than that in reality. Therefore it results in a better CRT than actually even possible. For the sampling intervals of 130 ps one can consequently find regions with a bigger CRT than possible ($\approx$ 230 ps) as shown in fig. 3.23(a). This also explains the other PMT result with the huge CRT fluctuation in the previous section 4.9.

Thus, X742 publications that predict revolutionary time resolutions have to be questioned and ideally repeated with comparable readout electronics. Due to the outcome of this thesis, this issue has been resolved starting with the fifth version of DRS4 Evaluation Board from PSI. However, the same mistake can still happen with older versions which should be replaced or upgraded according to section 2.2.9. This mistake probably also happened in the 2016 publication from Du et al[110] where a simple linear interpolation showed better time resolution compared to all presumably better timing methods.

4.11 CRT-Test of Reference PMT and MPPCs

Around 100 scintillation-photons with a decay time of 15 ns are expected from the $PbWO_4$-crystal (see table 1.1) which was utilized in this CRT-test (More experimental details are given in section 2.5.5). The $PbWO_4$-crystal was coupled to three different MPPCs. The best CRT for the MPPC2 (50 μm pitch) was around 670 ps (FWHM) as seen in table 3.11. This was achieved by triggering on the first photoelectron under the condition that more than 8 photons were detected in the rising edge of the signal. In rare cases 16 photoelectrons ($\approx \frac{130\,\mathrm{mV}}{8\,\mathrm{mV}}$) are measured for the MPPC2 as shown in fig. 3.44(d). Although the PDE of the MPPC3 is half that

of MPPC2, also around 16 photoelectrons are collected as the maximum value (see fig. 3.45). Thus, the faster recovery time causes the MPPC3 to collect the same amount as the MPPC2. MPPC1 shows a worse CRT compared to MPPC2 because around half the photoelectrons are collected as the maximum value (see fig. 3.43). The reduced number of photoelectrons stands in conflict with the highest available PDE in this CRT-test. The explanation is that the longest dead time in combination with the fewest micro pixels result in the lowest number of maximum photoelectrons.

The CRT of the MPPC3 cannot be compared to the other two measurements (MPPC1 & MPPC2) because the TH was accidentally set to around 200 mV. The high TH of 200 mV in combination with the narrow time window of 5 ns triggered events where the eighth photoelectron falls inside the provided time window. Therefore only selected PET-events were collected. This explains why the best CRT is measured for events where exactly 8 photoelectrons are collected. As listed in table 3.11, the best CRT for MPPC3 is calculated with a TH greater than 3 photoelectrons. The other two cases where the correct trigger settings were applied result in the best CRT when the arriving time is calculated for the first photoelectron.

Summarized, $PbWO_4$ results in a worse CRT compared to LSO. A good CRT depends on a fast rise time in combination with a high light yield. Thus, this outcome was predictable when looking at table 1.1 where LSO provides 380 ph/ns versus 7 ph/ns for $PbWO_4$.

Chapter 5

Conclusion

During the evaluation period several calibrations were developed which significantly improved the performance of the DRS4-chip. The DRS4 potential was wasted with regards to time resolution until the development of the new calibration (NEW-TC) which is highlighted in this thesis. The developer (PSI) of the DRS4 achieved with its original TC and a simple 2-points interpolation, a time resolution around 45 ps (σ) fluctuating between 27-52 ps. The fluctuation depends on the applied delays and additionally results in a non-Gaussian timing distribution. Instead the NEW-TC results in constant 3 ps (σ) when applying the same 2-points interpolation. Thus, one can say the NEW-TC enabled an error reduction by a factor of 15 for the DRS4. To be exact the error was reduced by more than 99.7 % (45 ps vs. $\sqrt{45^2 - 3^2}$ ps) since errors are expressed by the standard deviation. Further is evaluated in this work that the full performance of the DRS4 lies below 1 ps for more advanced interpolation techniques. Realized in this thesis is a single or unfolded time resolution below 580 fs ($\frac{0.82\,\mathrm{ns}}{\sqrt{2}}$) for the DRS4. This outcome inspired the group from Gary Varner, to discover the performance limits of the SCA technology. Their target is the 100 fs border[111].

Because of the demonstrated time resolution below 3 ps (σ), even between two individual running DRS4-chips, new opportunities have become available. PSI improved the multi-channel timing of the MEG experiment [87, 112]. Also PSI introduced a new evaluation board (V5) enabling precise time resolution measurements. An ideal field of application for the V5 are PET experiments. The older evalua-

tion boards can lead to wrong time resolution results especially for the interesting PET-timings below 200 ps (FWHM). This is also the case for the X742 from CAEN, which is the other DRS4-based board that was investigated. CAEN is aware of this issue and capable to recalibrate the X742. Summing up, old evaluation boards from PSI (before V5) and X742 boards can lead to better time resolution than actually even possible. This is the case for measurements in the time resolution region of 100-200 ps (FWHM), which is the region of the best reported time resolutions for PET.

Therefore, the results of this work are already of great benefit for the DRS4-based Whole-Body TOF PET at the University of Pennsylvania [113]. This DRS4-based PET proves that although this technology has a relatively high dead time, a fast PET picture can be generated with a smart trigger logic combined with an advanced PET design.

The investigated and improved readout electronics, the DRS4, gives the opportunity to measure accurately the individual errors of a PET-detector and to compare alternative readout electronics with each other. As a result the necessity of improvement for scintillator and photodetector is enabled by the fast readout electronics like the re-calibrated DRS4. Additionally, the NEW-TC can be applied to other SCA-chips, e.g. the PSEC4-chip[71] or the SAMPIC-chip[109], and thus offering the chance to improve their performance.

Appendix A

Scientific Publication and Patent

On the 8th of October 2013 an international patent application[95] "Verfahren zur Kalibrierung eines analogen Speicherarrays" was filed by the University of Tübingen. It contains the demonstrated new TC-methods for SCAs described in section 2.2. Since the 16th of April 2015 the patent application became available to the public under the international publication number WO 2015/051824. Additionally, a scientific publication from 2014 consisting of a simplified fraction of this work can be found in the following 11 pages. Chapter I – III of the following publication were written by Dr. Stefan Ritt. Figure 5 & 17 including its descriptions and discussions origin from Dr. Ritt. Figure 3 & 6 have been replaced by Dr. Ritt during the review process. The remaining content of chapter IV – VII and the abstract arose from the work of this thesis. In particular this includes all time calibration algorithms as well as the time resolution verification tests.

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Novel Calibration Method for Switched Capacitor Arrays Enables Time Measurements with Sub-Picosecond Resolution

D. A. Stricker-Shaver, S. Ritt and B. J. Pichler

***Abstract*—Switched capacitor arrays (SCA) ASICs are becoming more and more popular for the readout of detector signals, since the sampling frequency of typically several gigasamples per second allows excellent pile-up rejection and time measurements. They suffer however from the fact that their sampling bins are not equidistant in time, given by limitations of the chip process. In the past, this limited time measurements of optimal signals to standard deviations (σ) of about 4-25 ps in accuracy for the split pulse test, depending on the specific chip. This paper introduces a novel time calibration, which determines the true sampling speed of an SCA. Additionally, for two independently running SCA chips, the achieved time resolution improved to less than 3 ps (σ) independently from the delay for the split pulse test, when simply applying a linear interpolation. When using a more advanced analyzing technique for the split pulse test with a single SCA, this limit is pushed below 1 ps (σ) for delays up to 8 ns. Various test measurements with different boards based on the DRS4 ASIC indicate that the new calibration is stable over time but not over larger temperature variations.**

***Index Terms*—Time Calibration, DRS4, Switched Capacitor Array, Analog memory**

I. Introduction

SWICHED CAPACITOR ARRAYS (SCA) are application specific integrated circuits (ASIC) which allow transient analog signal recording at high sampling speeds. They have been first used for particle detector readout back in the 1980's as shown by Kleinfelder [1]. The principle is to use an array of capacitors in sample-and-hold mode. A fast sequence of write pulses allows the recording of analog waveforms in these capacitors, which can later be read out and digitized at a much lower speed. While early chips used shift registers to generate the write pulses, it was soon realized that using inverter chains as delay lines boost the sampling speed into the gigasamples per second (GSPS) region as demonstrated in [2]. Following the advances in CMOS technology, SCAs have become faster over the years, and current chip versions from different groups allow sampling speeds in the rage of 2-15 GSPS [3][4][5][6]. They have signal-to-noise ratios (SNR) of 10-13 bits equivalent and sampling depths of 256 to 64k cells. Paired with typical power consumptions of 10 mW per channel, these chips are excellent alternatives for commercial flash-ADCs. They all share however the disadvantage that the time required to read out the capacitor cells causes dead time. Depending on the number of channels and cells to read out, this dead time is in the typical rage of 1-100 micro seconds, which limits the application to cases where one can use a trigger to limit the number of events to typically 100-1000 events/s. The field of application for SCAs therefore lies in areas where one has a low trigger rate, but requires excellent time resolution and pile-up rejection. This includes for example particle physics at the intensity frontier[7], Cherenkov telescopes in gamma-ray astronomy[8], time-of-flight (TOF) applications [9] and neutrino physics[10]. Also, in medical imaging, specifically in positron emission tomography (PET), where TOF plays an important role[11], SCAs are a candidate for future applications. In [12] a coincident resolving time (CRT) of 100 ps (FWHM) was demonstrated for PET signals using $LaBr_3$ as a scintillator. This represents a single time resolution of ~30 ps (σ) and requires precise electronics to measure this time.

Several TOF measurements were made recently with various SCA chips. In the readout of micro channel plates, a single detector resolution of ~15 ps (σ) was achieved, which is comparable with the best commercial combination of constant-fraction-discriminators with time-to-amplitude converters, but at a much lower cost per channel [13]. The readout of straw tubes [14] via a time measurement gave good results, although the accuracy was limited by the imperfect time calibration (TC) method used for the SCA chip.

Over many years, the general opinion was that time measurements with SCA chips are limited to about 4-25 ps (σ) [6], caused by the time jitter inside the chips. The authors have found however that SCA chips can perform much better if the correct TC is applied. This allows pushing the achievable time resolution by about one order of magnitude to below one picosecond.

II. Theory of Operation

Most modern SCAs use a kind of inverter chain to generate the write pulses which open analog switches to sample the input signal. Fig. 1 shows a simplified schematics of the DRS4 chip, which is the fourth generation in a family of SCAs

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developed at PSI [5]. The advantage of this technique is that a simple inverter chain used as a tapped delay line can run much faster than any shift register, easily reaching 10-20 GSPS with modern chip technologies. The disadvantage however is that the transition time of an inverter depends on parameters like temperature and supply voltage. To address this problem, most SCAs use a delay-locked loop (DLL) or a phase locked loop (PLL) to stabilize the sampling frequency to an external constant reference clock.

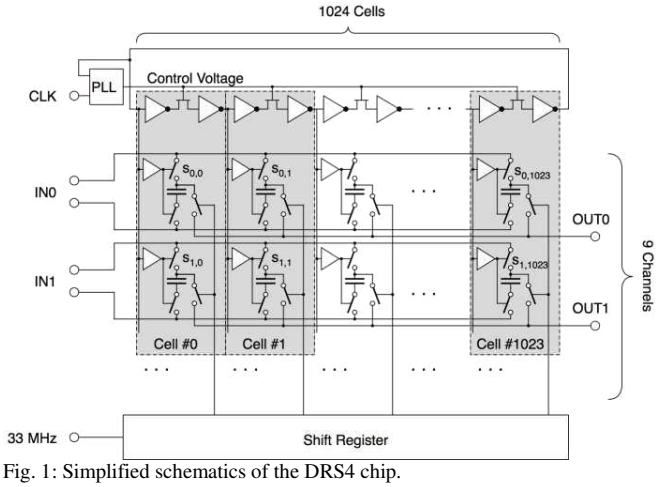

Fig. 1: Simplified schematics of the DRS4 chip.

Furthermore, mismatch between transistors in the CMOS process causes each inverter to have different but fixed transition times even if the other parameters are kept constant. Since this effect comes from the actual geometrical size of a transistor and its doping properties, it is stable over time and can be corrected for by measuring the transition time of each inverter and correcting for it. This measurement and its correction is the main topic of this paper and will be detailed in chapter IV.B.

III. Limitations of Time Measurements

After a proper TC, the accuracy of a time measurement with an SCA chip is limited by the residual random jitter of the transition time of the inverter chain. Each inverter has a voltage threshold at the input. Crossing this threshold turns the inverter high or low. While this threshold is very stable, any noise on the input signal will cause a time jitter of the inverter. Careful chip design allows minimizing this noise, causing modern SCA chips to have typical inverter chain time jitters below 1 ps.

To measure the arrival time of a certain electrical pulse e.g. in particle physics, the pulse time is typically extracted from the first rising or falling edge of the waveform, depending on the pulse polarity. The simplest case is to use a single threshold discriminator. In the case of waveform digitizing, the equivalent can be achieved in the digital domain by comparing the digitized voltage of the sampling points with a fixed value. To achieve a time resolution exceeding the sampling interval, adjacent samples can be interpolated linearly or with cubic functions. In Fig. 2a an interpolated line from an ideal signal intersects a given threshold at time t_1 depicted by an open square. Any voltage noise on the measured signal causes time jitter as shown in Fig. 2b. If some voltage noise "raises" the signal by an amount Δu, the linearly interpolated line intersects the same threshold at a time t_1' different from t_1, as depicted by the grey square. From Fig. 2b one can easily derive the formula for the time accuracy Δt as

$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}, \tag{1}$$

where U is the signal height, t_r the rise time and Δu the voltage noise as shown in Fig. 2.

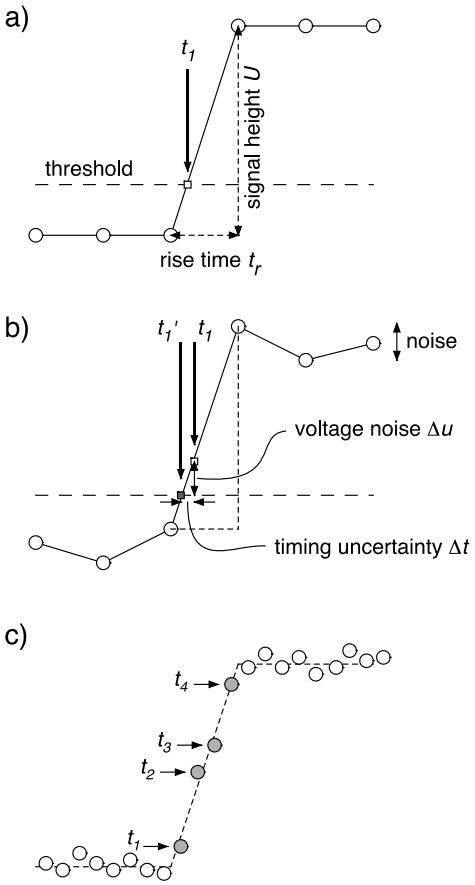

Fig. 2: Time estimations for a leading edge in the ideal case (a), in the presence of noise (b) and for several sampling points lying on the edge (c).

The time resolution can be improved by sampling the signal at a higher frequency. Fig. 2c shows the same signal sampled with four times higher sampling rate. The sampled points scatter around the signal indicated by the dashed line. Now several points lie on the signal edge, shown as grey circles. If the voltage noise of these points is statistically independent (as it is the case e.g. for ADC quantization noise), each point allows a separate measurement of the edge time, and thus reduces the time uncertainty of the edge by $\sqrt{n}$ where n is the number of points lying on the edge. The value of n is also determined by the product of sampling frequency f_s and the signal rise time t_r. This gives the theoretical time accuracy in dependence of the SNR which can be expressed as $U/\Delta u$,

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the sampling frequency f_s and the signal rise time t_r. Adopting this to (1) and solving for Δt gives

$$\Delta t = \frac{\Delta u}{U} \cdot t_r \cdot \frac{1}{\sqrt{n}} = \frac{\Delta u}{U} \frac{t_r}{\sqrt{t_r \cdot f_s}} = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}} \ . \quad (2)$$

From (2) it becomes clear that not only a high sampling frequency is important for a precise time measurement, but also the SNR and the signal bandwidth. It should be noted that (2) is only a simplified formula, since the actual resolution depends on the exact waveform shape and the noise spectrum. It is however a good estimator which has been verified by the authors and other groups[15].

For very fast detector signals, such as pulses from micro-channel plates (MCP) which can have t_r below 70 ps, the sampling gets limited by the bandwidth of the signal chain. The limiting factor can be a pre-amplifier, a long cable or the SCA chip itself, which is further detailed in [4]. The -3dB bandwidth f_{3dB} determines the signal rise time seen by the SCA as

$$t_r \cong \frac{1}{3 f_{3dB}} \ . \quad (3)$$

Putting this into (2) results in the time accuracy in dependence of the bandwidth f_{3dB} as

$$\Delta t = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}} = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}} \ . \quad (4)$$

Case	U (mV)	Δu (mV)	t_r (ns)	f_{3dB} (MHz)	f_s (GSPS)	Δt (ps)
a)	10	1	1	333	5	45
b)	450	1	1	333	5	1
c)	100	1	0.35	950	5	2.6
d)	500	0.35	1.6	-	5	0.5
e)	63	0.35	0.2	-	5	1.1

Table 1: Theoretical limit of the achievable time resolution Δt for certain signal and sampling parameters.

Table 1 lists various scenarios, which are relevant for this paper. Cases a) – c) assume a typical environmental or preamplifier noise Δu of 1 mV. The SCA internal noise in case of the DRS4 is 0.35 mV (case d) and e)). In all five cases the SCA is running at a sampling speed of 5 GSPS. Assuming a rise time of 1 ns, which is typical for many photomultipliers, it becomes clear that small signals in the 10 mV range will never give a time accuracy better than a few ten ps. Only a significantly higher signal – for example by means of a low-noise, fast preamplifier – can bring the resolution into the picosecond range. If one uses even faster pulses, the bandwidth gets limited by the SCA itself at some point. In the case of the DRS4 chip this bandwidth is 950 MHz, which limits the time resolution for a SNR of 100:1 to 2.6 ps (case c). Case d) and e) are relevant for the TC in chapter IV.B., which is performed with a 100 MHz sine wave with an amplitude of about 1V.

IV. Materials and Methods

The TC methods were evaluated with the DRS4 Evaluation Board version 3 (board A) with 12 bits, 5 GS/s and 4 channels provided by PSI[16] and the DRS4-chip based V1742 (board B) with 12 bits, 5 GS/s and 32 channels, provided by CAEN, Italy[17].

We further compared the performance results of board A & B with a LeCroy Wave Runner 6050A Oscilloscope (board C) with 8 bits, 5 GS/s and 4 channels and with the V1751 (board D) with 2 GS/s, 10 bits and 4 channels provided by CAEN. In this paper the presented measurements of board A, B and C were taken at a sampling speed of 5 GSPS, while board D used a sampling speed of 2 GSPS.

A. *Voltage Calibration*

Since voltage errors and time errors on an SCA chip are correlated, it is important to correct for any voltage error before a TC can be done. It consists of three corrections.

Firstly, the voltages of the stored waveform show slightly different offsets and gains for each sampling cell. In the DRS4 chip, this comes mainly from the fact that each sampling capacitor is read out by a separate buffer, which has a typical random offset of 10-20 mV. These offsets can be measured by connecting the input to a DC voltage, e.g. 0 V, and then subtracting these offsets in each measurement as an offset correction.

Secondly, a time-dependent readout offset correction is performed. This compensates for small supply voltage variations when the DRS4 chip is switched from sampling to readout mode. The different power consumptions of the DRS4 chip in these two modes causes a small dip in the power supply voltage, which cannot be recovered completely by the linear regulator or the blocking capacitors. The dip causes the DRS4 output to shift by about 2 mV for about 10 µs after it has been stopped.

Thirdly, the gain correction for each cell is done by applying a DC voltage of 800 mV to the input and measuring the response of the cell. The third correction is performed for board A but not for board B.

It is important to do the offset correction at the same voltage level as used later for time measurements, because the gain does not show an absolutely linear behavior. An example is given in Fig. 14, where for board B an external bias offset gets applied to shift the input range of the DRS4 chip after the voltage calibration.

Some SCA chips have the problem that some residual imprint of the previously stored signal distorts the last sampled waveform. This can cause the chip to respond differently to DC signals and to AC or transient signals. In the case of the DRS3 chip, this so-called “ghost pulses” could amount to 2-5 percent distortion of a waveform, depending on the sampling speed. This problem has been fixed for the DRS4 chip by issuing a clear cycle before a storage cell is written. Both sides of the storage capacitor are connected to ground by additional analog switches for a few nano seconds before every write cycle, thus removing efficiently any previously stored charge in the cell.

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B. Time Calibration (TC)

The sampling intervals of the DRS4 chip are not equidistant, but constant over time. This means the DRS4 has to be calibrated before a precise time measurement can be made. One can find such TC methods, e.g. in [6],[9],[18] and [16]. In this paper the new TC will be referred to as TC N. The time calibration from board A will be named TC A [16].

Consistently, the TC from board B will be called TC B. The TC B is unknown, since CAEN ships its boards already calibrated and nothing is mentioned in the manual.

In the following we will use Δt_i as the effective sampling interval between cell# *i* and cell# *i+1*. We define Δt_i as the time difference between the opening of the analogue switches $S_{0,i}$ and time point $S_{0,i+1}$ as illustrated in Fig. 1. From this follows that the integrated or "global" time difference between cell# k and cell# q is given by:

$$\Delta t_{k,q} = \sum_{i=k}^{(q-1)} \Delta t_i \,. \tag{5}$$

We digitized a known sine wave to perform TC N. The frequency of this sine wave $f_{\mathrm{TC\,N}}$ should be adjusted accordingly to the sampling speed range of the SCA. For the DRS4 sampling speed range of 0.7 - 5 GSPS , we recommend the frequency of 35 MHz in order to achieve best results. 35 MHz is the highest possible frequency due to (6) for the critical 0.7 GSPS case. If the sine frequency is much higher, the linear interpolation method would break down, if the frequency is lower, the duration of the TC would increase. Thus, TC N works in the frequency ranges

$$f_{\mathrm{TC\,N}} \in \left[\frac{2}{n}\cdot f_{SCA} \;,\; \frac{1}{20}\cdot f_{SCA}\right], \tag{6}$$

where f_{SCA} is the nominal sampling frequency of the SCA and n stands for the number of it cells.

In the following sections we always run the DRS4 at a sampling speed of 5 GSPS. For TC N we used the highest frequency we had available to reduce calibration time. We therefore used a sine wave of 100 MHz with an 1 V peak-to-peak amplitude, which is the middle range of (6).

TC N consists of two parts. The first part estimates the effective sampling intervals Δt_i by measuring voltage differences between two neighboring cells and is called "local" TC. The second part refines the sampling intervals by measuring time differences between cells that are far apart and is therefore called "global" TC. While the local TC effectively corrects the differential time non-linearity, the global TC reduces the integral time non-lineariy as will be shown later in Fig. 5.

1) Local TC

Two publications ([9],[19]) have already introduced the basic idea that we call the local TC. We devolved this idea independently and combining it with our global TC described later, which would improve the current results significantly as in Fig. 5.

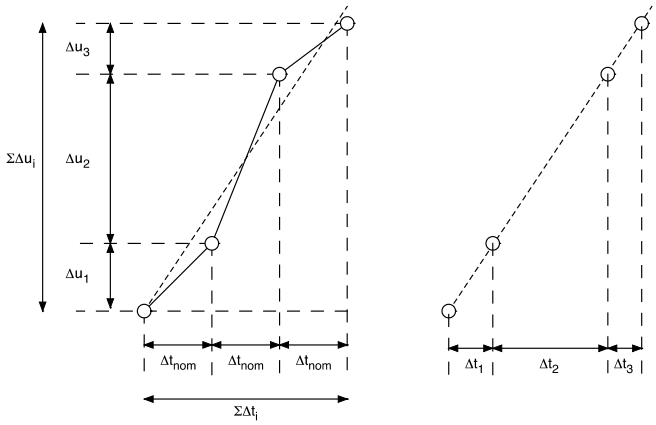

Fig. 3: The correlation between voltage differences Δu_i and time differences Δt_i of a rising edge can be used for the local TC of an SCA chip.

The approach is that Δt_i is proportional to the measured voltage difference between neighboring cells when applying a linear increasing or decreasing signal, such as a saw-tooth waveform for example. The intercept theorem results in (7) and is illustrated in Fig. 3:

$$\frac{\Delta t_i}{\Delta U_i} = \frac{\sum \Delta t_i}{\sum \Delta U_i}, \tag{7}$$

where ΔU_i is the voltage difference between cells *i* and *i+1*. For an SCA with *n* cells we know

$$\sum_{i=1}^{n} \Delta t_i = \frac{n}{f_{SCA}} \,. \tag{8}$$

When combining (7) and (8), we can calculate all n time intervals Δt_i as:

$$\Delta t_i = \frac{\Delta U_i \cdot \frac{n}{f_{SCA}}}{\sum \Delta U_i} \,. \tag{9}$$

The exact sampling speed of the SCA that might deviate from f_{SCA} is not required since it will be determined in the global TC afterwards.

Using rising and falling edges of the TC signal will result in two calibrations. Averaging over these two calibrations will cancel any residual voltage offset:

$$\Delta t_i = \left(\Delta t_{i,falling} + \Delta t_{i,rising}\right) \cdot \frac{1}{2}, \tag{10}$$

where $\Delta t_{i,falling}$ and $\Delta t_{i,rising}$ stand for the time differences calculated by the falling and rising edges, respectively. Tests have indicated that using the rising and falling edges of a sine wave like the one in Fig. 4 are good enough to obtain an acceptable local TC. In a digitized waveform only the Δt_i for cells on the slopes of the sine wave can be determined. The procedure therefore has to be repeated for several sine waves with a random phase relative to the SCA clock. 1000 digitized sine waves give a decent result for the local TC when simply using the arithmetic mean values.

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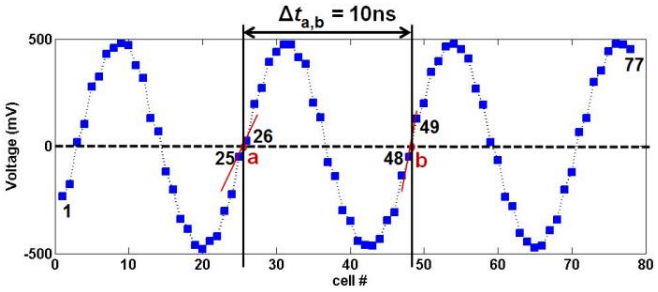

Fig. 4: First 77 cells of the 1024 cell array of a DRS4 sampling a 100 MHz sine wave at a sampling speed of 2.5 GSPS. This signal is used for the local TC and the global TC.

For the 5GSPS case, the local TC is using sampling points in the range of ± 100 mV.

2) Global TC

The global TC measures one or more periods of the 100 MHz sine wave. The period is determined by linearly interpolating sampling points below and above zero volts and measuring the time between the intersections of the interpolated lines with the zero line as shown in Fig. 4. In this example the zero crossing is between cells #25 and #26 and between cells #48 and #49, leading to two corrections

$$t_{cor} = \frac{U_k}{\Delta U_{k-1}} \Delta t_{k-1} - \frac{U_q}{\Delta U_q} \Delta t_q \,, \tag{11}$$

which constrain the time between the cell# k = 26 and cell# q = *48* using the known period time of $f_{\mathrm{TC\,N}}$ as in

$$m \cdot \frac{1}{f_{\mathrm{TC\,N}}} \overset{\mathrm{def}}{=} t_{k,q} + t_{cor} \quad , \tag{12}$$

where m stands for the factor describing the multiples of the measured periods. U_i is the voltage measured at cell# i.

In Fig. 4 the global time difference $\Delta t_{a,b}$ has to be $1 \cdot 10$ ns. The two points a and b are artificial points and stand for the zero crossings of two rising edges of the digitized sine wave.

Finally the global TC is computed iteratively by correcting the local TC each time we measure a multiple of the period time $m \cdot 1/f_{\mathrm{TC\,N}}$.

$$\begin{aligned} \Delta t_{k,\mathrm{new}} &= \Delta t_k \cdot u_{cor} \\ \Delta t_{k+1,\mathrm{new}} &= \Delta t_{k+1} \cdot u_{cor} \\ &\vdots \\ \Delta t_{q-1,new} &= \Delta t_{q-1} \cdot u_{cor} \end{aligned} \quad \text{with} \quad u_{cor} = \frac{m}{f_{\mathrm{TC\,N}} \cdot (t_{k,q} + t_{cor})} \,, \tag{13}$$

where $\Delta t_{k,new} \ldots \Delta t_{q-1,new}$ stand for the corrected effective sampling interval. $\Delta t_k \ldots \Delta t_{q-1}$ stand for the old data set of effective sampling intervals that are going to be corrected. The first iteration will start with the data set provided by the local TC (9). In the following iterations the $\Delta t_{i,new}$ provided by (13) will be retitled in Δt_i in order to apply (13) again every time a new $t_{k,q}$ is measured. Iterating over typically 1000 digitized sine waves is usually enough to obtain a precise global TC. Ideally one should treat falling and rising edges separately and determine the global TC after applying (10). For practical reasons, the measured sine waves in the local TC can be "recycled" for the global TC. In Table 1 case e) one can see that the expected time resolution is about 1.1 ps for a single interpolation. In this case the voltage difference between sampling points of a rising edge is in average about 63 mV with an average sampling interval of 0.2 ns.

The error arising from the linear interpolation of the sine wave is predictable and can be estimated. Simulations for an expected sampling interval of 0.2 ns show that the global TC error is less than 0.08 ps, and less than 0.7 ps in the worst case scenario, where some sampling intervals could vary up to 0.4 ns. Increasing the TC frequency will increase the maximum error of the global TC.

The global TC improves the local TC for two reasons. First, the local TC is never perfect. Any measurement has a statistical error, which accumulates if one integrates over many measurements. Second, the SCA cells have different effective analog bandwidths along the chip. The cells close to the input pin see a smaller resistance of the signal bus inside the chip than the cells far away from the input pin. This causes slightly different rise times for the calibration sine wave in different cells, and causes a systematic error for the local TC, which is then removed efficiently by the global TC.

C. Board Time Resolution Tests

To examine the time resolution of the four boards and the quality of TC N, 4 different performance tests were applied. The time resolutions for all performance tests are given as standard deviation (σ) and refer to resolution on time difference. All these σ values were extracted from a Gaussian fit applied to their distributions. The σ coming from the fit is insensitive to appearing outliers, which are typically less than 0.1 % of all measurements. The value of a calculated standard deviation (often the terminology root-mean-square (RMS) is used) compared to σ received from the fit was never more than 0.2 ps increased. An example is given in the section Results in Fig. 13.

1) The Period Time Test (PT-test)

The 100 MHz sine wave used for the TC N is also used for the PT-test. Fig. 5 shows the measured period time between two zero crossings of the rising edges, which should be equal to 10 ns. The period time is plotted over the cell number that is left of the first zero crossing. Thus, $\Delta t_{\mathrm{a,b}}$ from Fig. 4 would be represented by cell# 25 in Fig. 5. The top plot shows the time for an uncalibrated DRS4 chip, the middle after the local TC and the bottom after the global TC. While the local TC effectively corrects variations between neighboring cells, a residual inaccuracy with more global structures is left over, which can be seen in the middle plot. The global TC then corrects these global structures, which leads to a flat distribution shown in the bottom plot. This method is therefore very powerful to determine the accuracy of a TC.

In Table 2 we compare the distribution of the period time (i.e. the projection of the distribution in Fig. 5 bottom onto the Y-axis) for different hardware. For each measurement, 10000 events were digitized and averaged. When digitizing the 100 MHz sine wave with 5 GSPS, we measured average voltage

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difference between two consecutive samples of ΔU_i= 63 mV around the zero crossings. This effective signal height was used to predict the result of the SP-test by using (1).

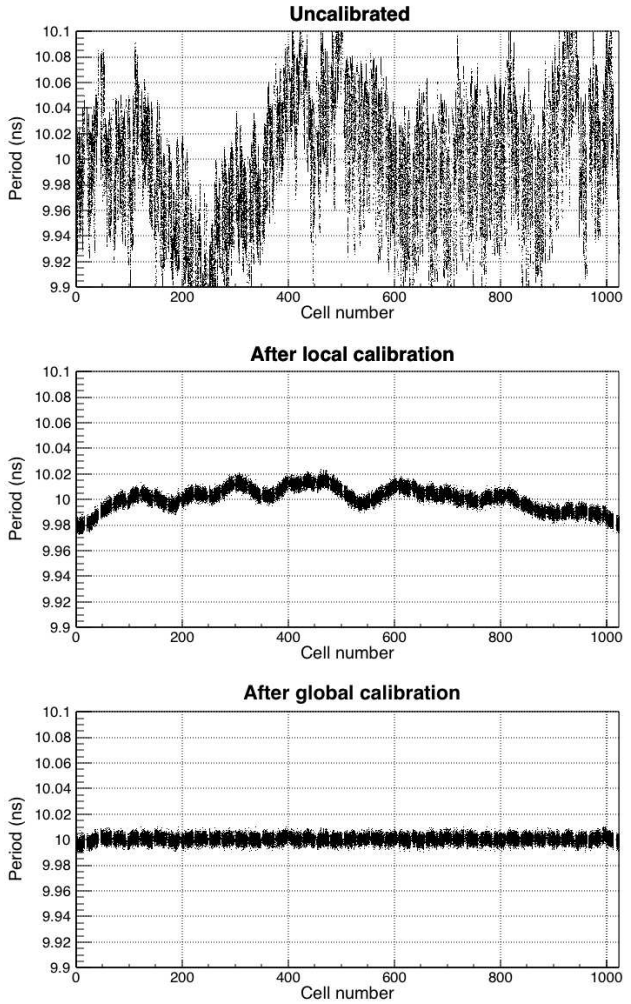

Fig. 5: Effect of the local TC and the global TC when used to determine the period of a 100 MHz sine wave (PT-test).

2) The Split Pulse Test (SP-test)

We evaluated the actual time precision for the tested boards as shown in Fig. 6a with the SP-test. A short pulse is generated by a function generator. The signal is split and the time difference between the arrivals of the two signals is measured. We changed the arrival time of one of the signals by applying a variable cable delay (Fig. 6a and Fig. 7).

In most cases we used a simple Digital Leading Edge (DLE)-discriminator to evaluate the time resolution. This means, we interpolated between two points of the rising edge to obtain the time information at a given threshold. A global threshold (TH) of 300 mV was used for all SP-tests (Fig. 7). In Fig. 10 and Fig. 14 the THs were changed individually for a single SP-test measurement (50 ns cable delay) resulting in a time resolution matrix. One can see that the global TH of 300 mV is a good compromise for all SP-test that use a DLE-discriminator.

The time resolution improves by using more points. Thus, we also performed the SP-test with a DLE-discriminator by fitting though 6 points of the rising edge.

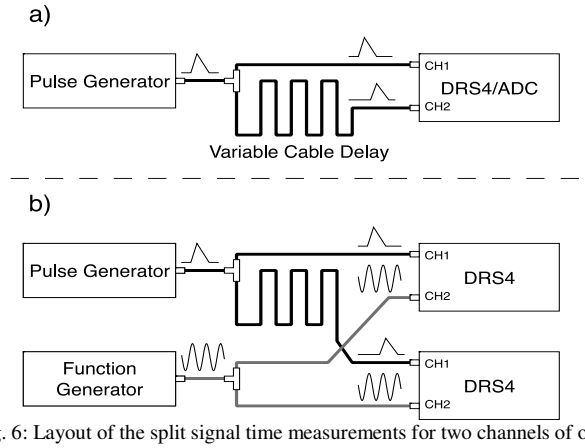

Fig. 6: Layout of the split signal time measurements for two channels of one chip (a) and between two chips synchronized by a sine wave (b).

Best results for the SP-test were achieved by cross-correlating both channels. In this case all non-baseline related sampling points of the pulse were used. Thus, we used 50 points of the split signals. Before, 50 linear interpolations were made for each channel in order to result in equidistant sampling points.

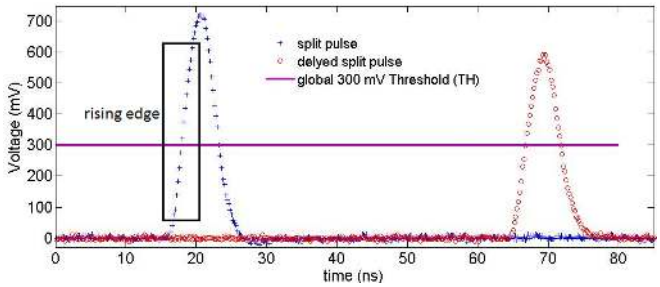

Fig. 7: Split pulse digitized at 5 GSPS for the SP-test with board C and a full range of ~1.1V. The left signal height peaks around 720 mV and the delayed signal peaks at around 610 mV due to cable attenuation. The time difference between the signals is approximately 50 ns. The split pulse rise time is around 3 ns or 15 sampling points.

Also the time resolution (σ) between two independently running DRS4 chips was tested (Fig. 6b). In this case a 100 MHz clock was split and additionally sampled in a separate channel in each of the chips. The measured phase shift of the split clock was used to synchronize the two DRS4 chips.

3) The Coincident Resolving Time Test (CRT-test)

Fig. 8 shows the setup of a PET time resolution measurement (CRT) when using the DRS4 chip with and without applying TC N instead of TC B. We used two 5mm · 5mm · 5mm LSO:Ca crystals as scintillators glued to two fast PMTs (Hamamatsu R10560). The Results are displayed in a matrix form, where the time resolution (σ) is given as a function of the thresholds for both PMT channels. The thresholds are measured in % of the averaged 511keV photo-peak height of the individual channel.

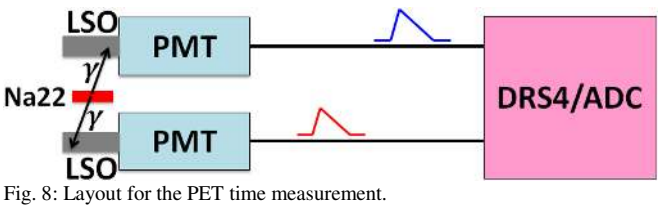

Fig. 8: Layout for the PET time measurement.

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4) The Temperature Time Dependence Test (TTD-test)

For the TTD-test board A was used. When performing the TC N, 10 global time differences $\Delta t_{1,100}$ to $\Delta t_{900,1000}$ were measured at 8 different temperature levels in 5 °C steps from 5 °C to 40 °C. Aftereach temperature change, board A had to run 12 hours in a temperature controlled box before the TTD-test was performed. The temperature was measured with two sensors, one located in the box and the one included in board A. The temperature on the board was larger in average by 12°C compared to the box temperature due to the self-heating of the board.

V. Results

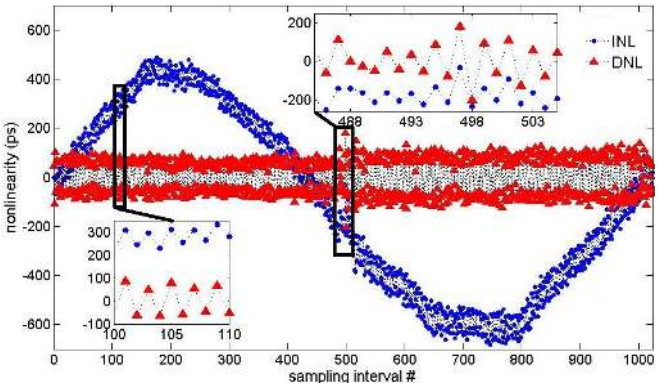

Fig. 9: Integrated nonlinearity (INL) and differential nonlinearity (DNL) of all sampling intervals measured by TC N for channel# 4 of board A running at 5 GSPS.

An alternating sampling behavior was expected when looking at the slopes of the waveform in Fig. 4. The sampling intervals of adjacent cells differ alternating by about 70 ps for the DRS4 from the nominal width of 200 ps at 5 GSPS, which can be seen in Fig. 9. The integrated nonlinearity (INL) varies in this case from -680 ps to 486 ps. The differential nonlinearity (DNL) is alternating stronger and has extremes at interval# 497 = 170 ps and interval# 498 = −203 ps. The DNL smaller than -200 ps means that the signal reaches cell# 499 always 3 ps before it gets sampled in cell# 498 which can be explained by the layout of the chip. The input bus is routed due to some constraints such that the signal reaches cell #499 before it reaches cell #498. From 20 tested DRS4 chips, cell# 498 was the only cell showing this behavior and is typically in the DNL range of -205 ps and -150 ps when sampling at 5 GSPS.

By using the TC N we also verified that board B is running at the nominal 5 GSPS. We evaluated that all previous versions of the DRS4 evaluation boards version 5, such as board A, were running at 5.1206 GSPS instead of the expected 5.1200 GSPS.

1) The Period Time Test (PT-test)

Table 2 shows among others the results for the oscilloscope (board C). The resolution can be improved by increasing the gain, but with the drawback of a clipped signal. The full 100 MHz 1 V signal was only visible in the first case on the oscilloscope screen and results for channel# 2 in a time resolution of 16.7 ps (σ). By increasing the gain the information of the full waveform got lost but increased the SNR and therefore increased the time resolution. The best gain uses the 8 bits for a full range of 112.5 mV and achieved a time resolution of 3.6 ps (σ). Increasing the gain further would cause some loss of information at the zero crossings and degrade the resolution again.

Table 2 shows that board A gives a better time resolution for the PT-test than board C. Both boards show the expected period time of about 10 ns.

One can also see that TC N is about 15 times better than TC A and also provides the correct period time of 10 ns, even when TC N for channel# 1 is applied to channel# 2.

Additionally, it demonstrates that every channel has to be calibrated individually to obtain a time resolution below 10 ps.

2) The Split Pulse Test (SP-test)

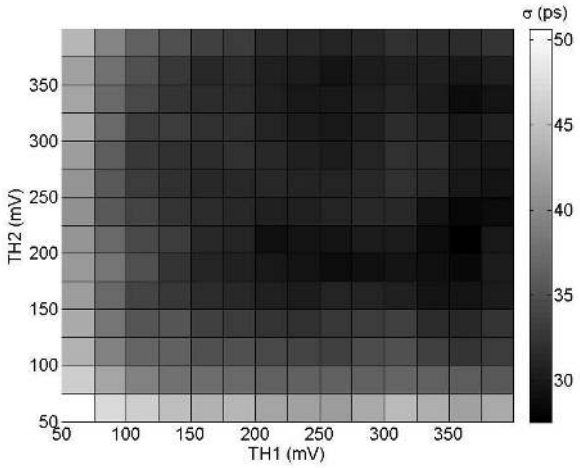

Fig. 10: SP-test (2 points) obtained with board C with 50 ns delay. The optimal TH settings of TH1 = 350 mV and TH2 = 200 mV give a time resolution of 28 ps (σ).

The results for the SP-test of a 50 ns delay are shown in Fig. 10 and Fig. 14. Fig. 10 shows the time resolution result of the SP-test for board C in dependence on the first threshold TH1 (first signal) and the second threshold TH2 (second signal) of the used digital leading edge (DLE) discriminator. The optimum time resolution is 28 ps (σ) with the signal shown in Fig. 7, which was digitized with 8 bit resolution and a full range of ~ 1.1V.

Fig. 11 illustrates results of a SP-test, where the time resolution in dependency of the delay is shown. Board D (large crosses) was running at 2 GSPS with a resolution of 10 bits. The two other boards were running at 5 GSPS using the DRS4 chip. The x-symbols mark the results of Board A using TC A and indicate a time resolution variation from 25 ps to 55 ps (σ). The same board achieves a time resolution of about 3 ps (σ) for all delays when TC N was applied (circles). The dots stand for the measurement points of board B using TC B. The 2-point-DLE-discriminator was used in all four cases.

Fig. 12 shows a zoom-in of the board A (TC N) curve from Fig. 11. For the same dataset two additional analysis methods are also shown. The circles and the dots were calculated with a DLE-discriminator. For the 50-point measurement (crosses) the cross-correlation method was used. One can see that the time resolution progresses when using more points. The time resolution curve shows approximately a linear rising behavior for this three cases.

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used board	used time calibration	$\frac{1}{SNR} = \frac{\Delta u}{U^*}$ $(*\approx 63\,mV)$ ch1	ch2	Mean Value (ps) ± σ (ps) [expected σ with (1)] (ps) ch1	ch2
C	-	0.0827	0.0702	10000.9 ±20.80[23]	10000.0 ±16.70 [20]
C	-	0.0163	0.0138	10000.1 ± 5.20[4.6]	10000.0 ± 4.60 [4.0]
C	-	0.0090	0.0076	10000.1 ± 3.90[2.5]	10000.0 ± 3.60 [2.1]
A	TC N for each ch#	0.0068	0.0071	10000.0 ± 3.11[1.9]	10000.0 ± 3.23 [2.0]
A	TC N (always ch1)	0.0068	0.0071	10000.0 ± 3.11[1.9]	10000.0 ±13.20 [2.0]
A	TC A	0.0068	0.0071	10004.5 ±48.05[1.9]	10003.2 ±52.11 [2.0]

Table 2: PT-test results for board A with 3 different TC & board C with 3 different gains. The theoretical best time resolution according to formula (1) is shown in brackets.

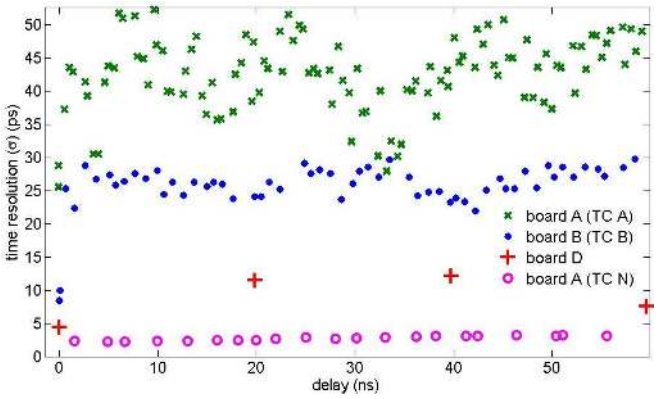

Fig. 11: SP-test measurements (2 points) obtained for 3 different boards.

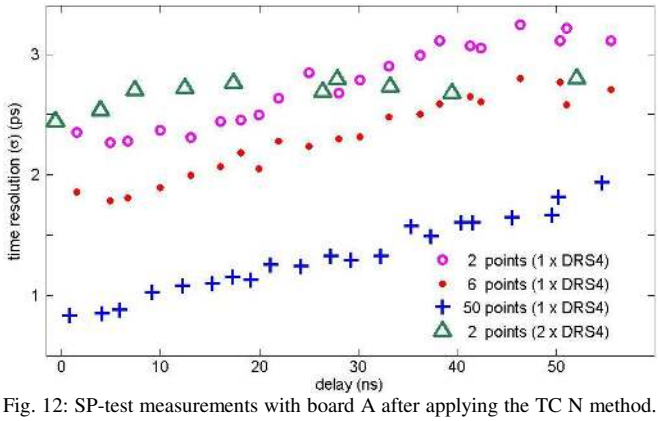

Fig. 12: SP-test measurements with board A after applying the TC N method. The triangles show the SP-test results of two independently running boards A, where a 2-point-DLE-discriminator was used. For the other 3 curves, where the SP-test was performed only with one board A, the same dataset was analyzed three times using different analyzing techniques.

The triangles in Fig. 12 demonstrate the time resolution results of the SP-test for two independently running boards A, synchronized by a dedicated split clock as described previously (Fig. 6b). The DLE-discriminator using only 2 points results in a time resolution better than 2.8 ps (σ) for all delays. The best achieved time resolution between two independently running DRS4 chips when using cross-correlation was better than 1.65 ps (σ) for any delay.

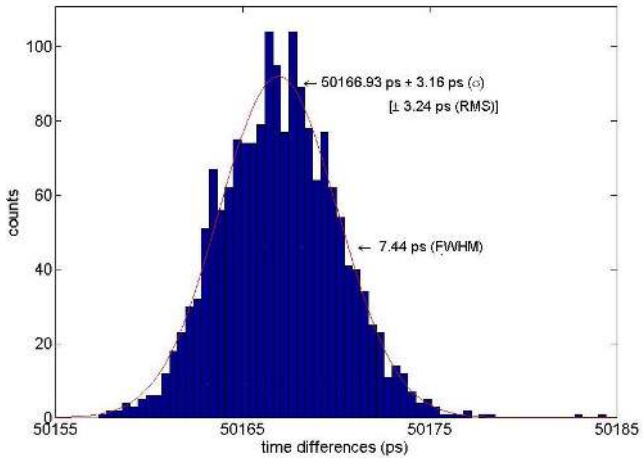

Fig. 13: SP-test distribution for the 2-point-DLE-discriminator (second to last triangle from Fig. 12).

Fig. 13 demonstrates a single time resolution result of the SP-test from Fig. 12. A delay of about 50 ns was used and all measured 2000 events were plotted. One can see two outliers appearing at the right side.

The effect of using the wrong offset correction level with the DRS4 is illustrated in Fig. 14. The same experimental setup as shown in Fig. 7 is now digitized with 12 bit resolution. Additionally, we shifted intentionally the baseline by applying a 400 mV DC offset. The time resolution of board B as shown in Fig. 14 for a given TH of 300mV is 4.6 ps (σ) when using TC N. As expected the best TH2 level is lower than the optimal TH1 level, since the split signal is 15 % smaller in the second channel. When running the DRS4 of board B at the optimal DC offset level and applying the gain correction for board B one will result in 3ps (σ) as shown for board A in the 50 ns delay case of Fig. 11.

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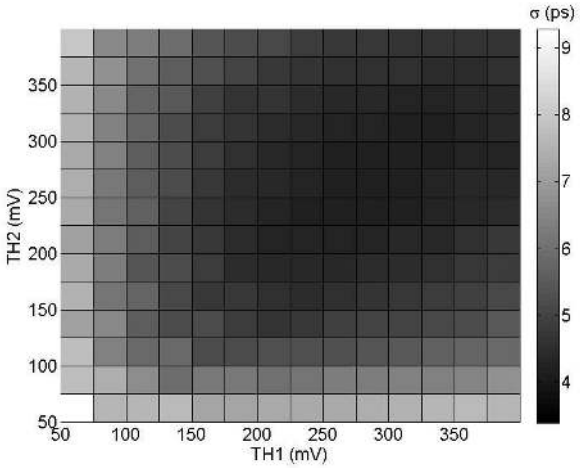

Fig. 14: SP-test (2 points) with the same delay as in Fig. 10 for board B. The optimal TH settings TH1 =275mV and TH2=250mV give a result of 4.4ps (σ).

3) *The Coincident Resolving Time Test (CRT-test)*

Fig. 15 shows two time resolution results of the CRT-test as a function of the thresholds TH1 (PMT# 1) and TH2 (PMT# 2) of the used 2-point-DLE discriminator. TH1 and TH2 are given in percentage of the average photo peak height of the particular channel. 65 ps CRT (σ) with TC B for best THs was measured and 74 ps CRT (σ) with the TC N. See Discussion for more details.

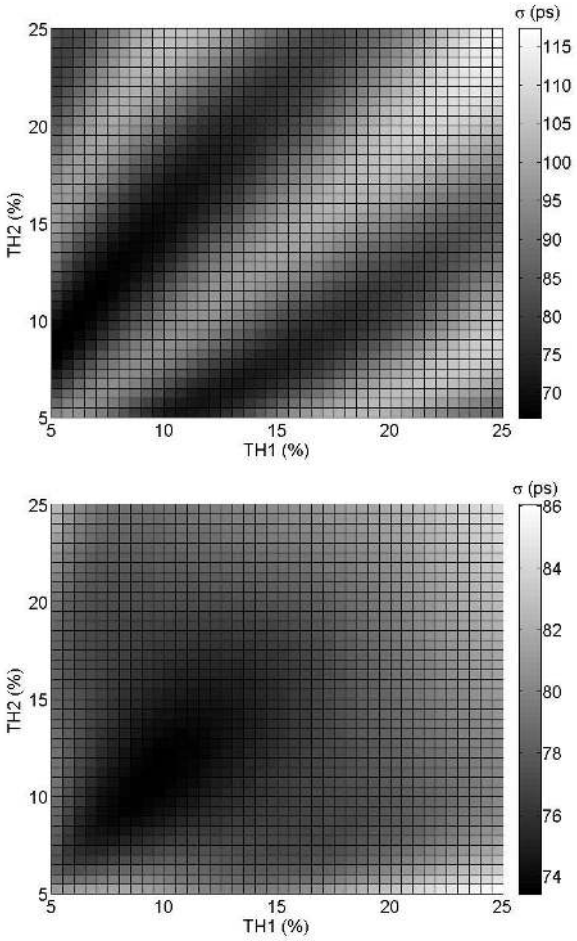

Fig. 15: Results for the CRT-test measured with board B. Two measurements with changing from TC B (top) to TC N (bottom) were performed.

4) *The Temperature Time Dependence Test (TTD-test)*

In Fig. 16 the temperature dependency of the time resolution of the DRS4 chip is plotted. One can see that half of the $\Delta t_{a,b}$ are varying less than 2 ps. However $\Delta t_{1,100}$ shows a maximum change of -12 ps compared to the 5°C case. The ten regions summed together result in no time change, indicating that the sampling speed remained stable. The reason for the temperature dependence is not completely clear, but can to some part be contributed to gradients of transistor parameters along the chip wafer.

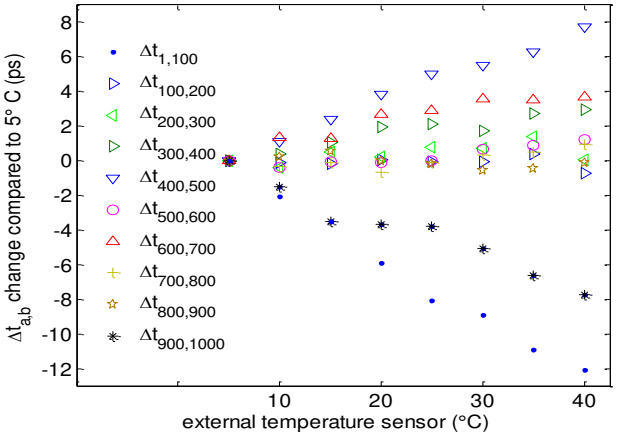

Fig. 16: TTD-test of board A. For each of the 8 measurements 1000 digitized waveforms were analyzed. Ten global time difference $\Delta t_{a,b}$ are showed in 20 ns steps. All $\Delta t_{a,b}$ values are around 20 ns and were subtracted from its corresponding 5°C case to illustrate the influence of temperature change for the DRS4. .

VI. Discussion

Previous TCs, like TC A and TC B, predicted not-alternating Δt_i of 200 ps with an σ of 4 ps. By using TC N for the DRS4 chip we discovered that the true value of the sampling intervals Δt_i alternate between 130 ps and 270 ps with a σ of ~23 ps at 5 GSPS (Fig. 9). The reason for these alternations lies in the layout of the DRS4 chip. The 1024 sampling cells of one channel are not linearly arranged, but folded due to the limited size of the die. This causes odd and even cells to see a different environment on the chip and to be differently connected to the power rails. At lower sampling speeds one will find a similar alternating behavior of the DRS4 chip. Since the signal edges between the inverters have longer rise times at lower sampling speed, internal noise plays a bigger effect and the timing performance degrades about inversely with the sampling frequency $\Delta t \sim 1/f_s$.

1) *The Period Time Test (PT-test)*

The PT-Test in Table 2 shows that TC N for board A yields in the expected period time of 10 ns and a time resolution of 3.1 ps. With the best gain, board C only reaches 3.6 ps. Since the time resolution is proportional to the rise time of the signal at a given signal-to-noise, a higher gain setting for board C results in a better time resolution, although the peaks of the test-signal will then be clipped.

The channel-by-channel TC (illustrated in Table 2) can be

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understood by looking at Fig. 1. Every analog switch connected to the sampling capacitors has a separate buffer. The transition times of these buffers are different due to the above-mentioned variations in chip process parameters.

Board A had issues before with measuring long time differences ([20] and Fig. 11). This problem is now understood and has several reasons. The reasons will be addressed in decreasing significance. First, the TC frequency that was used for TC A had a 120 ps time jitter with a non-Gaussian distribution. Second, the true sampling intervals alternate and do not show a 200 ps ± 4ps behavior as predicted by TC A & B, but a 200 ps ± 74 ps behavior. Third, for every channel of an SCA chip an individually TC is mandatory. Fourthly, the true sampling speed differed from the expected sampling speed by about 0.01 %. The measurement of the true sampling speed with TC N and the usage of a more precise oscillator with less jitter on version 5 of board A solved this problem. Fifthly, a 2.5 MHz digital signal on board A on a PCB trace close to the DRS4 chip induced some instability of the PLL inside the DRS4 which lead to two distinguished alternating sampling speeds. A redesign of the PCB with better shielding of this signal fixed that problem.

2) The Split Pulse Test (SP-test)

Looking at the 50 ns delay result from Fig. 12 compared to Fig. 14 shows a time resolution degradation from 2.9 ps to 4.6 ps for the same measurement when using a different offset level and no gain correction. We used a DLE-discriminator where the stability of the baseline is mandatory. This underscores that the cell-to-cell gain spread leading to level-dependent offsets up to 0.5 mV (see data sheet [21], Plot 2) has a considerable effect on the time resolution. A cell-by-cell calibration of the non-linearity could therefore improve the time resolution even further.

Under similar conditions (Fig. 7) board C achieved 28 ps(Fig. 10). This was predictable since it only uses 8 bits for a full range of ~1.1V. The best time resolution for board C performing the SP-test was around 8 ps, when the gain was increased by a factor of 10 to a full range of 0.1125V, but with the penalty of above-mentioned clipping.

Fig. 11 shows the SP-test for different boards and TCs. In comparison to TC B the TC A on board A is about two times worse. This is mainly caused by the TC-signal that was used for the TC A, which has a jitter greater than 100 ps. Also, the time resolution should remain constant when increasing the delay, which is not the case for TC A or TC B. Instead, the DRS4 digitizers show a strong correlation between the delay and its corresponding time resolution behavior when using TC A or TC B.

The large DRS4 time resolution improvement when comparing TC N with the other TCs can be explained with the following: when looking at the time axes of an uncalibrated channel running at 5 GSPS, the maximal error is around 800 ps. When comparing TC N with TC A or TC B, the maximum error is still around 150 ps. This is because the other TCs provide almost equidistant sampling intervals of 200 ps with a σ of 4 ps and not the alternating behavior mention at the beginning of section VI. However, one can also see in Fig. 11 that after using TC N, the curve for board A lies below the curve of board D as expected, because the DRS4 was running at 5 GSPS using 12 bits and board D at 2 GSPGS using 10 bits.

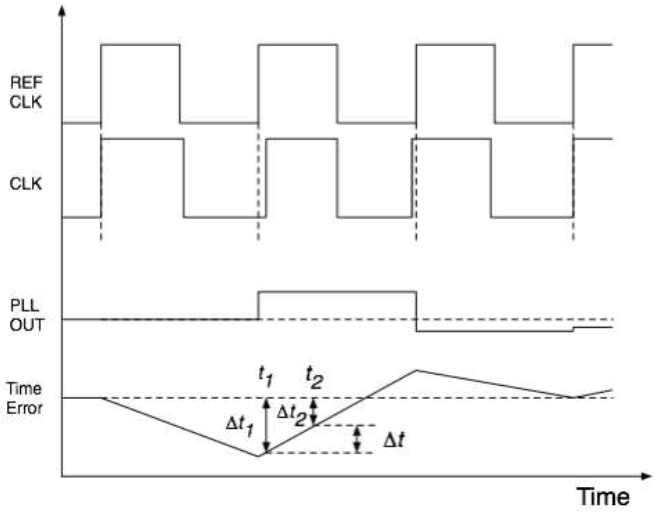

Fig. 17: PLL phase jitter in an SCA chip. REFCLK is the external (exact) reference clock, CLK the frequency of the inverter chain, PLLOUT is the control voltage from the PLL and Time Error the deviation of the sampling time from the exact time.

In Fig. 12 one can see that the time resolution is improved by using more sampling points of the signal, as expected. We observe however even for short delays an improvement by less than $1/\sqrt{n}$, which has three reasons. Firstly, the 2-point measurement used the samples with the best SNR (the highest slope of the signal), so the other sampling points will contribute less to the improvement of the measurement. Secondly, the measured samples are not statistically independent as required by the $1/\sqrt{n}$ law. This comes from the fact that the noise spectrum of the measured signal has slower components, which can affect adjacent samples in a coherent way. Thirdly, the linear interpolation is not the optimal fitting method.

The increase of the time resolution with the cable delay comes from the fact that the sampling speed varies around its nominal value due to the residual phase jitter of the PLL in the DRS4 chip. This can be seen in Fig. 16 which shows the deviation of the sampling time from the exact time due to the PLL time jitter. If two signals are sampled at times t_1 and t_2 on separate channels driven by the same inverter chain, their deviation from the perfect time is Δt_1 and Δt_2, respectively. The relative time error between the two signals is Δt, which is proportional to the time distance $t_2 - t_1$ as long as the time difference is smaller than the clock period. Since the inverter chain in case of the DRS4 is 1024 cells long, the time resolution in Fig. 13 increases from 0.8 ps at 0 ns delay (which is close to the theoretical optimum) to 4.8 ps at 200 ns delay (extrapolated), reflecting the PLL jitter of about 4 ps.

Fig. 12 also shows that this increase of the time resolution with the cable delay can be compensated by the additional sampled 100 MHz clock information that was used to

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synchronize two DRS4 chips. As expected the time resolution of the SP-test is worse compared to the single DRS4 case for short delays. On the other hand, cable delays above 25 ns already result in better time resolution and were measured for cable delays up to 150 ns to be less than 2.8 ps (σ).

3) The Coincident Resolving Time Test (CRT-test)

In Fig. 15 the importance of applying TC N is shown with an example of a real PET measurement (Fig. 8). Looking at measurements of board B using TC B one will get a wrong result. This is illustrated in the top figure of Fig. 15, which shows 3 minima instead of just one expected and is 7 ps better CRT (σ) than possible. We know that the time resolution result of board B (TC B) is wrong because we double checked the experiment with an oscilloscope with 20 GSPS and an adjusted gain for a comparable 12 bit resolution. Although we digitized 4 times faster, we only archived a CRT (σ) of 72 ps for best threshold (TH) settings.

The reason for the wrong result is the following:

We know that the effective sampling interval Δt_i of TC B provides almost equidistant 200 ps sampling intervals. As mentioned above the true Δt_i alternates between 130 ps and 270 ps. When changing the TH settings as shown Fig. 15 one will also measure different time differences between the two PET signals (walk effect). The three minima also represent regions of similar time differences. When this time difference is calculated by interpolating between two neighboring cells that are mainly 270 ps apart but wrongly considered to be 200 ps, the calculated σ will be smaller than in reality and will therefore result in a wrongly considered as better time resolution result. Considering sampling intervals of around 130 ps one will also find regions with bigger time resolution than possible as shown in Fig. 15.

4) The Temperature Time Dependence Test (TTD-test)

The temperature stability test of board A in Fig. 16 shows that the variation of $\Delta t_{a,b}$ with the temperature is less than 1-2 ps in a temperature range from 5°C to 10°C. However, the variation of $\Delta t_{a,b}$ cannot be ignored for bigger temperature variations. $\Delta t_{200,700}$ can be predicted by summing the corresponding $\Delta t_{a,b}$ from Fig. 16 and results in an expected change of 23 ps for $\Delta t_{200,700}$ when increasing the temperature by 35° C. For temperature changes around 1-2 °C the $\Delta t_{a,b}$ variation is below the extrapolated PLL jitter of around 2 ps for this delay. Thus, a temperature adjusted TC is mandatory if an excellent time resolution is needed and if the temperature varies more than 2°C. However, the TC was tested to be valid over several months. Also the sampling frequency stays the same for the tested temperatures as shown in Fig. 16 when adding all 10 temperature points together.

VII. Conclusion

The novel TC N gives excellent results for DRS4-based time measurements. Since the limitations of time measurements are very similar in most SCA chips, such as unequal propagation times of inverter chains and buffers, it is very likely that this calibration is well applicable also for other SCA chips.

In the DRS4 case a time resolution improvement by a factor of 8 to 15 has been achieved (Fig. 11). The performance is now much better compared to an oscilloscope, while the costs of an SCA-based system are one order of magnitude lower. For a single DRS4, up to 30 ns delay (Fig. 12), the SP-test using cross-correlation is below 1.4 ps (σ), giving a single time resolution better than $1.38\,\text{ps}/\sqrt{2} = 0.98\,\text{ps}$ (σ). However, when performing the SP-test on two independently running DRS4 chips and using a simple 2-point-DLE-discriminator, a single time resolution better than $2.80\,\text{ps}/\sqrt{2} = 1.98\,\text{ps}$ (σ) was achieved for any cable delay.

Thus, the DRS4 provides an excellent measurement platform for applications in particle physics or in PET medical imaging.

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We would like to thank the University Hospital Tübingen for making it possible to file in an international patent application (No. PCT/EP2013/070892) containing several TCs including the demonstrated new TC method.

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